

MBR3520
MBR3535
MBR3545, H, H1

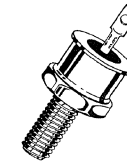
SWITCHMODE POWER RECTIFIERS

using a platinum barrier metal in a large area metal-to-silicon power diode. State-of-the-art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free-wheeling diodes, and polarity-protection diodes.

- Guardring for dv/dt Stress Protection
- Guaranteed Reverse Surge Current/Avalanche
- 150°C Operating Junction Temperature

SCHOTTKY BARRIER RECTIFIERS

35 AMPERES
20 to 45 VOLTS



CASE 56-03
DO-203AA
METAL

MAXIMUM RATINGS

Rating	Symbol	MBR3520	MBR3535	MBR3545, H, H1*	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	35	45	Volts
Peak Repetitive Forward Current (Rated V_R , Square Wave, 20 kHz, $T_C = 110^\circ\text{C}$)	I_{FRM}	70			Amps
Average Rectified Forward Current (Rated V_R , $T_C = 110^\circ\text{C}$)	$I_{F(AV)}$	35			Amps
Peak Repetitive Reverse Surge Current (2.0 μs , 1.0 kHz) See Figure 8	I_{RRM}	20			Amps
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	600			Amps
Operating Junction Temperature	T_J	-65 to +150			$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +175			$^\circ\text{C}$
Voltage Rate of Change (Rated V_R)	dv/dt	1000			V/ μs

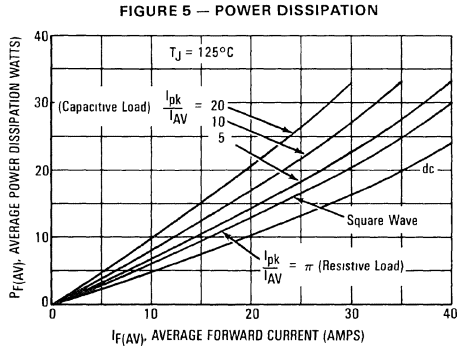
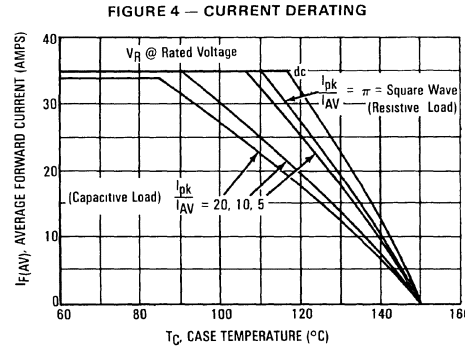
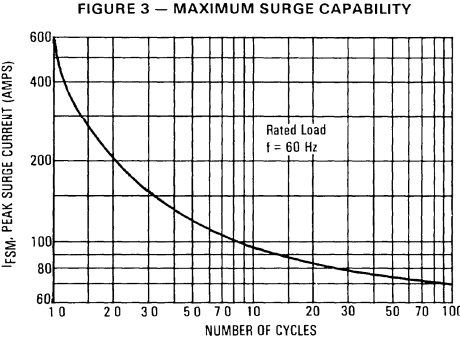
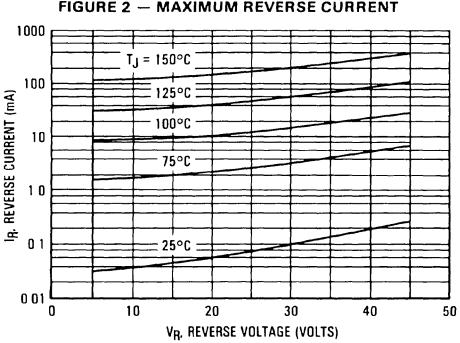
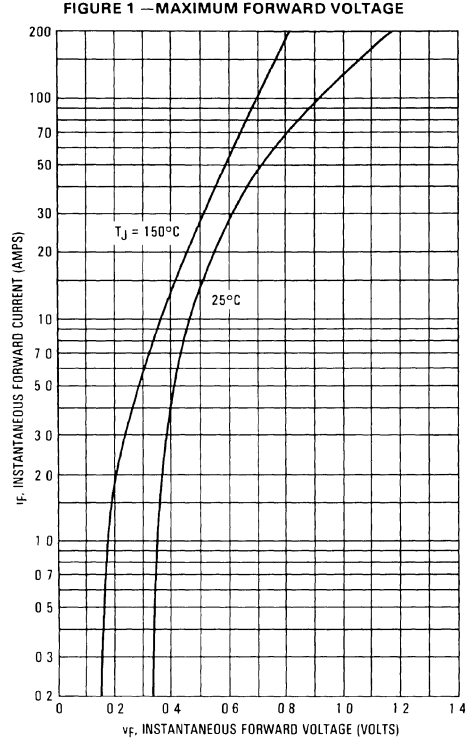
THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.3	1.5	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS PER DIODE

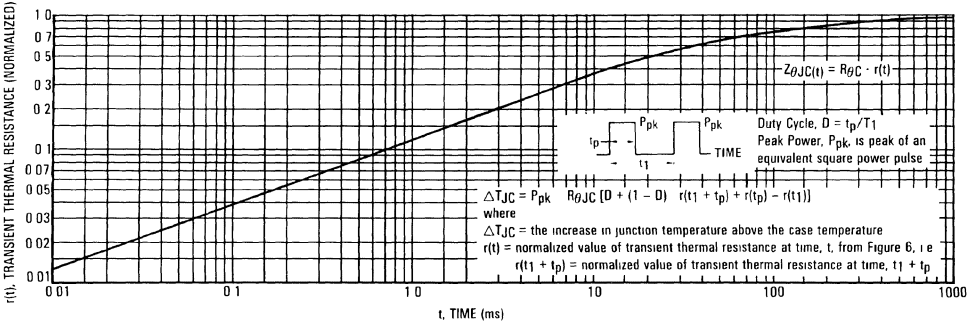
Characteristic	Symbol	Typ	Max	Unit
Instantaneous Forward Voltage (1) ($I_F = 35$ Amp, $T_C = 125^\circ\text{C}$) ($I_F = 35$ Amp, $T_C = 25^\circ\text{C}$) ($I_F = 70$ Amp, $T_C = 125^\circ\text{C}$)	V_F	0.49 0.55 0.60	0.55 0.63 0.69	Volts
Instantaneous Reverse Current (1) (Rated Voltage, $T_C = 125^\circ\text{C}$) (Rated Voltage, $T_C = 25^\circ\text{C}$)	I_R	60 0.1	100 0.3	mA
Capacitance ($V_R = 1.0$ Vdc, 100 kHz $> f >$ 1.0 MHz, $T_C = 25^\circ\text{C}$)	C_t	3000	3700	pF

*H and H1 devices include extra testing. See Figure 10.
(1) Pulse Test. Pulse Width = 300 μs , Duty Cycle = 2.0%



3

FIGURE 6 — THERMAL RESPONSE



3

HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 7.)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss, it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

FIGURE 7 — CAPACITANCE

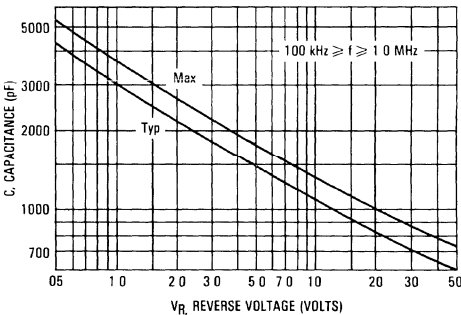
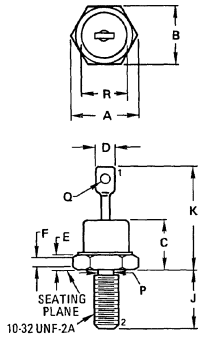
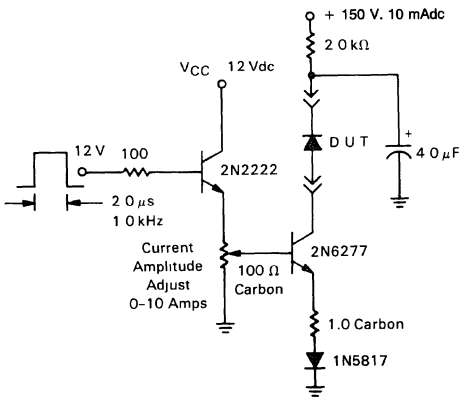


FIGURE 8 — TEST CIRCUIT FOR dv/dt AND REVERSE SURGE CURRENT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.94	12.83	0.470	0.505
B	10.77	11.10	0.424	0.437
C	—	10.29	—	0.405
D	—	6.35	—	0.250
E	1.91	4.45	0.075	0.175
F	1.52	—	0.060	—
J	10.72	11.51	0.422	0.453
K	—	20.32	—	0.800
P	4.14	4.80	0.163	0.189
Q	1.52	—	0.060	—
R	—	10.77	—	0.424

All JEDEC dimensions and notes apply

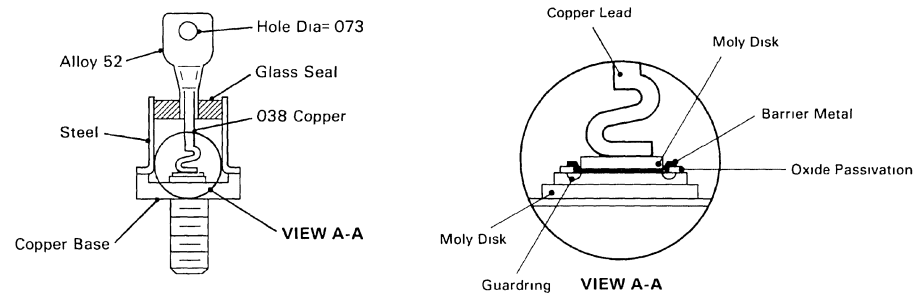
STYLE 2
TERM 1 ANODE
2 CATHODE

CASE 56-03
DO-203AA
METAL

MOUNTING TORQUE: 15 in-lb max

MBR3520, MBR3535, MBR3545, H, H1

FIGURE 9 — SCHOTTKY RECTIFIER



Motorola builds quality and reliability into its Schottky Rectifiers

First is the chip, which has an interface metal between the platinum-barrier metal and nickel-gold ohmic-contact metal to eliminate any possible interaction with the barrier. The indicated guardring prevents dv/dt problems, so snubbers are not mandatory. The guardring also operates like a zener to absorb over-voltage transients.

Second is the package. There are molybdenum disks which closely match the thermal coefficient of expansion of silicon on each side of the chip. The top copper lead is also stress-relieved to prevent damage during assembly. These two features give the

unit the capability of passing powered thermal fatigue tests for 5,000 cycles. The top copper lead provides a low resistance to current and therefore does not contribute to device heating, a heat sink should be used when attaching wires.

Third is the redundant electrical testing. The device is tested before assembly in "sandwich" form, with the chip between the moly disks. It is tested again after assembly. As part of the final electrical test, devices are 100% tested for dv/dt at 1,600 V/μs and reverse avalanche. Devices are also 100% reverse scope tested for trace anomalies.

3

FIGURE 10 — HI-REL PROGRAM OPTIONS

