16384 WORD x 1 BIT DYNAMIC RAM

N CHANNEL SILICON GATE MOS

TMM416P/D-2, TMM416P/D-3, TMM416P/D-4

DESCRIPTION

The TMM416P/D is a 16,384 words by 1 bit MOS random access memory circuit fabricated with TOSHIBA's double poly N-channel silicon gate process for high performance and high functional density

The TMM416P/D uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation Multiplexed address inputs permit the TMM416P/D to be packaged in a standard 16 pin plastic and cerdip DIP This package size provides high system bit densities and is compatible with widely available automatic testing and insertion equipment

FEATURES

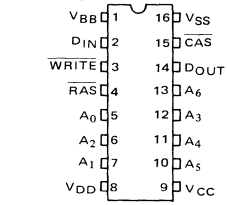
- 16,384 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{RC}
TMM416P/D-2	150 ns	320 ns
TMM416P/D-3	200 ns	375 ns
TMM416P/D-4	250 ns	410 ns

- Industry standard 16 pin DIP
- Standard ± 10% power supply (+12V, ± 5V)
- Lower power 462mW operating (max)
  20mW standby (max)
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using "Early Write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles / 2 msec
- Compatible with MK4116
- Package
  Plastic DIP TMM416P
  Cerdip DIP TMM416D

PIN CONNECTIONS

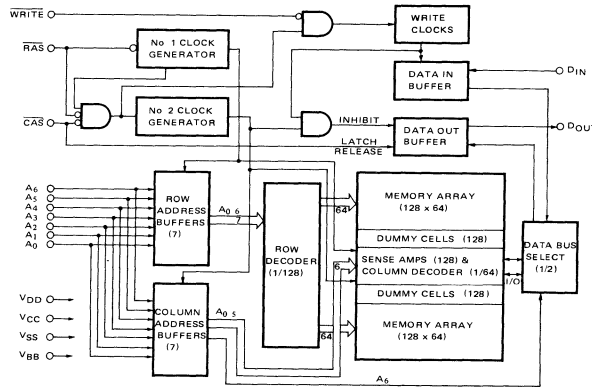
(TOP VIEW)



PIN NAMES

A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING		VALUE	UNITS	NOTES
Voltage on any pin relative to V_{BB}		−0.5 ~ +20	V	1
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}		−1.0 ~ +15	V	1
V_{BB}-V_{SS} (V_{DD}-V_{SS} ≥ 0V)		0	V	1
Operating temperature		0 ~ 70	°C	1
Storage temperature		−55 ~ 150	°C	1
Soldering temperature Time		260 10	°C sec	1
Power dissipation	TMM416P	600	mW	1
	TMM416D	1000		
Short circuit output current		50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C) (Note 2)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	3
V_{CC}		4.5	5.0	5.5	V	3,4
V_{SS}		0	0	0	V	3
V_{BB}		−4.5	−5.0	−5.5	V	3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	V	3
V_{IH}	Input High Voltage, except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	V	3
V_{IL}	Input Low Voltage, all inputs	−1.0		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, Ta = 0°C ~ 70°C) (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
I_{DD1}	OPERATING CURRENT		35	mA	5
I_{CC1}	Average power supply operating current				6
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = minimum value)		200	μA	
I_{DD2}	STANDBY CURRENT		1.5	mA	
I_{CC2}	Power supply standby current	−10	10	μA	
I_{BB2}	($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)		100	μA	
I_{DD3}	REFRESH CURRENT		27	mA	5
I_{CC3}	Average power supply current, refresh mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC} t_{RC} = minimum value)		200	μA	
I_{DD4}	PAGE MODE CURRENT		27	mA	5
I_{CC4}	Average power supply current, page mode operation				6
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = minimum value)		200	μA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = −5V 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0V)	−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	−10	10	μA	
V_{OH}	OUTPUT LEVELS Output "H" level voltage (I_{OUT} = −5mA)	2.4		V	4
V_{OL}	OUTPUT LEVELS Output "L" level voltage (I_{OUT} = 4.2mA)		0.4	V	4

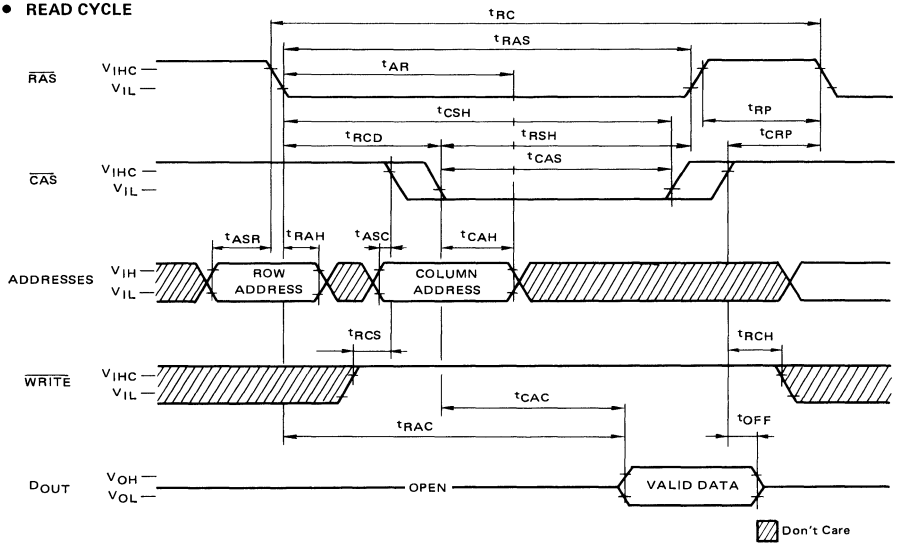
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, Ta = 0°C ~ 70°C) (NOTES 2, 7, 8, 10)

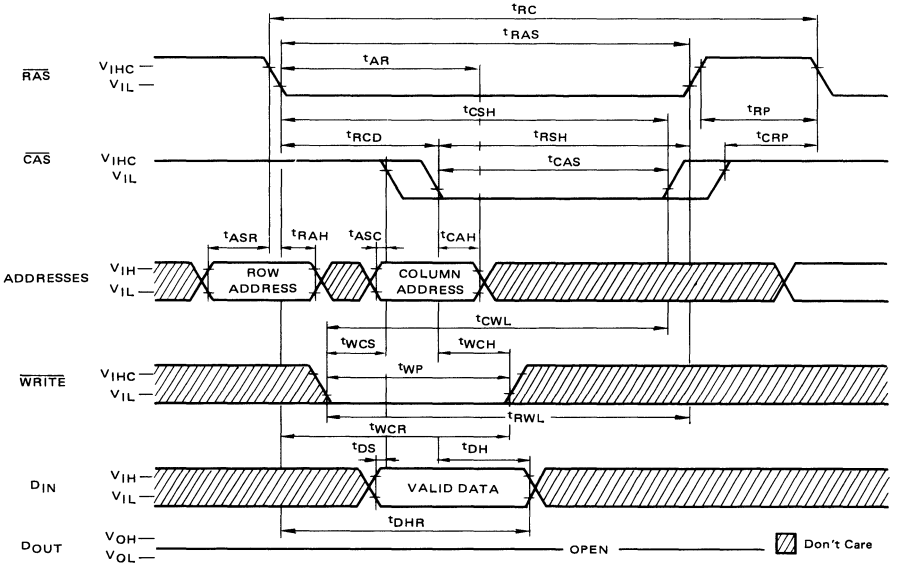
SYMBOL	PARAMETER	TMM416P/D-2		TMM416P/D-3		TMM416P/D-4		UNITS	NOTES
		MIN	MAX	MIN	MAX.	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read-modify-write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	11, 13
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	12, 13
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	14
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	10
t_{RP}	$\overline{RAS}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	32,000	200	32,000	250	32,000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	25	65	35	85	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	−20		−20		−20		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	20		25		35		ns	
t_{ASC}	Column Address set-up time	−10		−10		−10		ns	
t_{CAH}	Column Address hold time	45		55		75		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	16
t_{DH}	Data-in hold time	45		55		75		ns	16
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	−20		−20		−20		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	17

TIMING WAVEFORMS

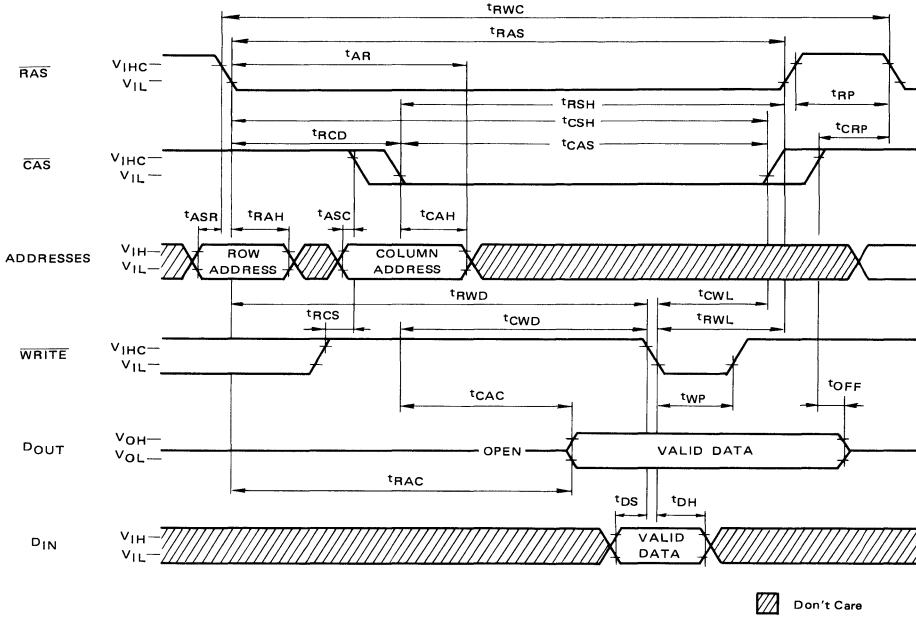
- **READ CYCLE**



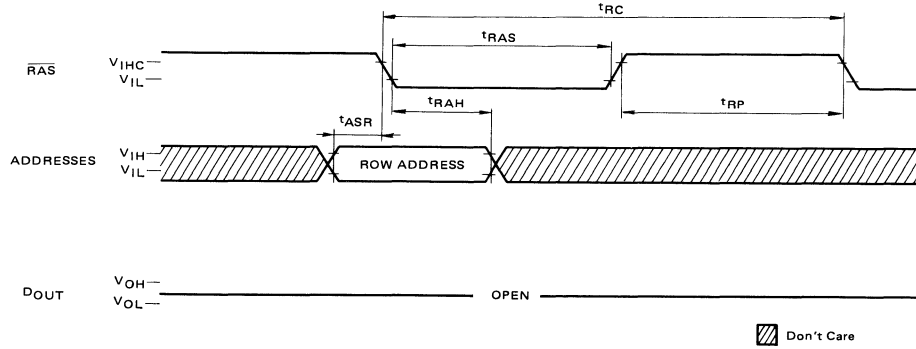
- **WRITE CYCLE (EARLY WRITE)**



- **READ-WRITE/READ-MODIFY-WRITE CYCLE**

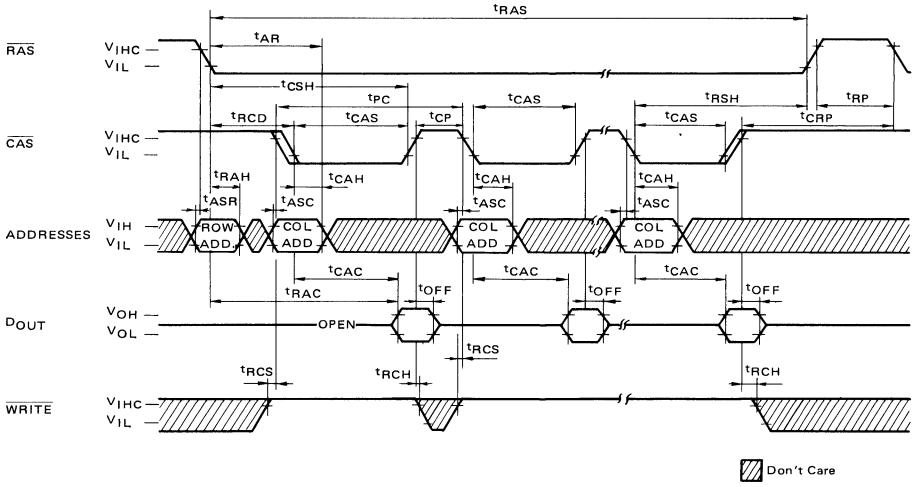


- **"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE**

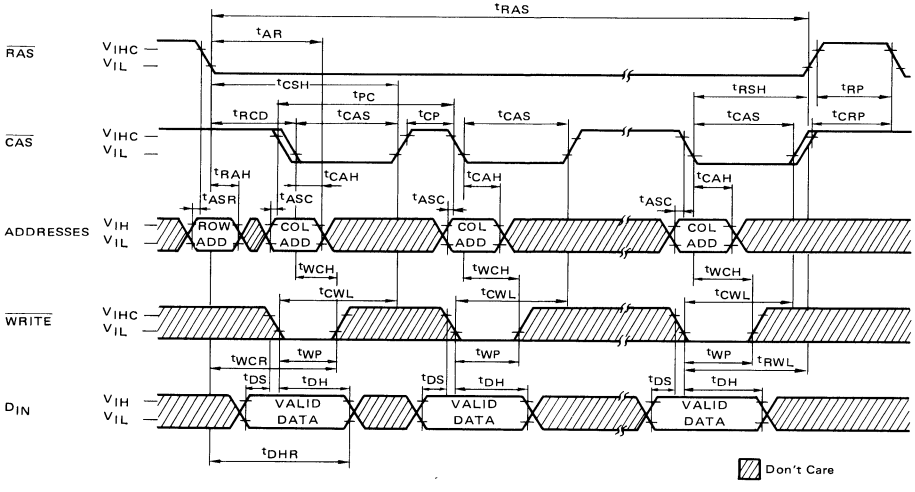


Note $\overline{\text{CAS}}$ = V_{IHC}, $\overline{\text{WRITE}}$ = Don't Care

- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



CAPACITANCE

(V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, f = 1MHz, Ta = 0°C ~ 70°C)

SYMBOL	PARAMETER	TYP	MAX	UNIT
C_{I1}	Input Capacitance (A_0-A_6), D_{IN}	4	5	pF
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF
C_O	Output Capacitance (D_{OUT})	5	7	pF

POWER DERATING CHARACTERISTICS

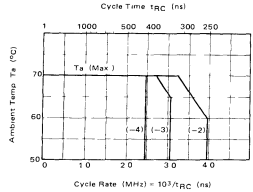


Fig 1 Ta vs t_{RC}

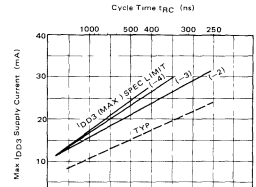


Fig 3 t_{RC} vs I_{DD3}

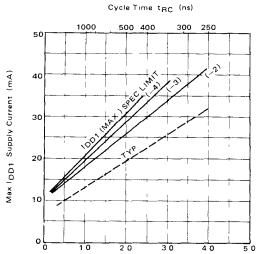


Fig 2 t_{RC} vs I_{DD1}

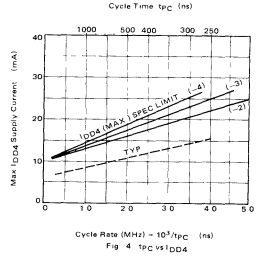


Fig 4 t_{PC} vs I_{DD4}

NOTES

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device

2 T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min) Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met See Fig 1 for derating curve

3 All voltages are referenced to V_{SS}

4 Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention However, the V_{OH} (min) specification is not guaranteed in this mode

5 I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate See figures 2, 3 and 4 for I_{DD} limits at other cycle rates

6 I_{CC1} and I_{CC4} depend upon output loading During readout of high level data V_{CC} is connected through a low impedance to data out At all other times I_{CC} consists of leakage currents only

7 After the application of supply voltages or after extended periods of bias (greater than t_{REF} 2ms) without clocks, the device must perform about eight initialization cycles prior to normal operation

8 AC measurements assume t_T = 5ns

9 The specifications for t_{RC} (min), t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured

10 V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

11 Assumes that $t_{RCD} \leq t_{RCD}$ (max) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown

12 Assumes that $t_{RCD} \geq t_{RCD}$ (max)

13 Measured with a load equivalent to 2 TTL loads and 100pF

14 t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels

15 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met t_{RCD} (max) is specified a reference point only if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

16 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles

17 t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters They are included in the data sheet as electrical characteristics only

If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle

If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate

APPLICATION INFORMATION

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the TMM416P/D are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register This permits several options in the write cycle timing In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$ If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM416P/D is the high impedance (open-circuit) state That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell This output data is the same polarity (not inverted) as the input data Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle)

PAGE MODE OPERATION

The "Page-Mode" feature of the TMM416P/D allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power This is done by

strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$ Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power This reduction in power is reflected in the I_{DD3} specification

POWER CONSIDERATIONS

Most of the circuitry used in the TMM416P/D is dynamic and most of the power drawn is the result of an address strobe edge (refer to the TMM416P/D current waveforms in Fig 5) In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the TMM416P/D can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in Fig 2

It is possible to operate certain versions of the TMM416P/D family (−2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met Operation at shorter cycle times (< t_{RC} min.) results in higher power dissipation and, therefore, a reduction in ambient temperature is required Refer to Fig 1 for derating curve

POWER UP

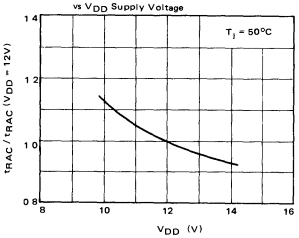
The TMM416P/D requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, TOSHIBA recommends sequencing of power supplies such that V_{BB} is applied first and removed last V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}

TYPICAL CURRENT WAVEFORMS

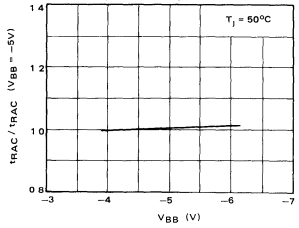
Fig 5

TYPICAL CHARACTERISTICS

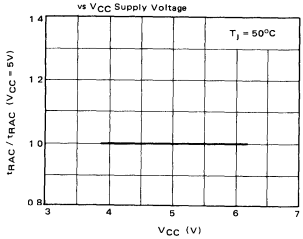
Normalized Access Time t_{RAC} vs V_{DD} Supply Voltage



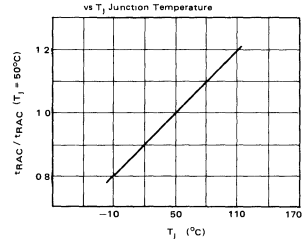
Normalized Access Time t_{RAC} vs V_{BB} Supply Voltage



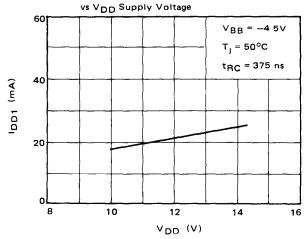
Normalized Access Time t_{RAC} vs V_{CC} Supply Voltage



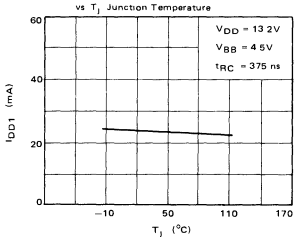
Normalized Access Time vs T_j Junction Temperature



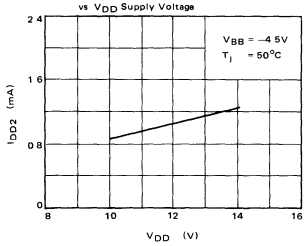
I_{DD1} (Average) vs V_{DD} Supply Voltage



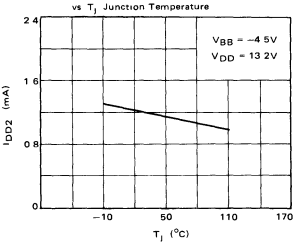
I_{DD1} (Average) vs T_j Junction Temperature



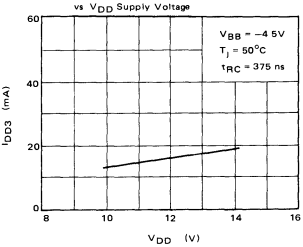
I_{DD2} (Standby) vs V_{DD} Supply Voltage

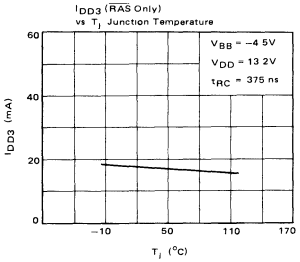


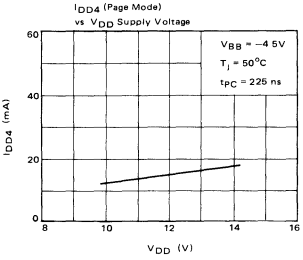
I_{DD2} (Standby) vs T_j Junction Temperature

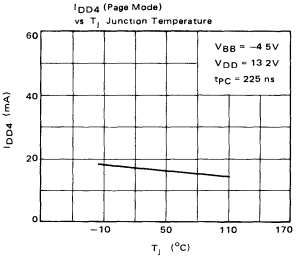


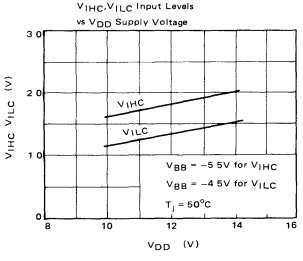
I_{DD3} ($\overline{RAS}$ Only) vs V_{DD} Supply Voltage

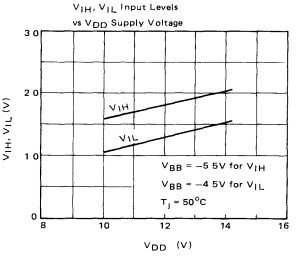


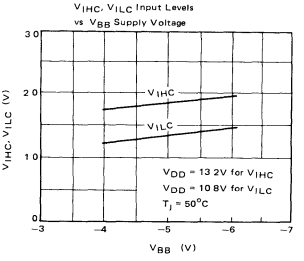

I_{DD3} ($\overline{RAS}$ Only)
vs T_j Junction Temperature
V_{BB} = −4 5V
V_{DD} = 13 2V
t_{RC} = 375 ns
I_{DD3} (mA)
60
40
20
0
−10
50
110
170
T_j (°C)

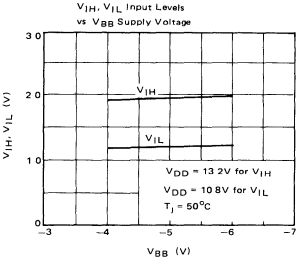

I_{DD4} (Page Mode)
vs V_{DD} Supply Voltage
V_{BB} = −4 5V
T_j = 50°C
t_{PC} = 225 ns
I_{DD4} (mA)
60
40
20
0
8
10
12
14
16
V_{DD} (V)

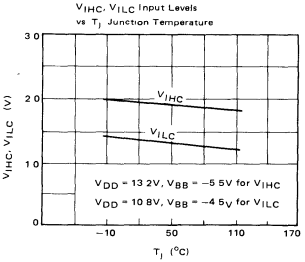

I_{DD4} (Page Mode)
vs T_j Junction Temperature
V_{BB} = −4 5V
V_{DD} = 13 2V
t_{PC} = 225 ns
I_{DD4} (mA)
60
40
20
0
−10
50
110
170
T_j (°C)

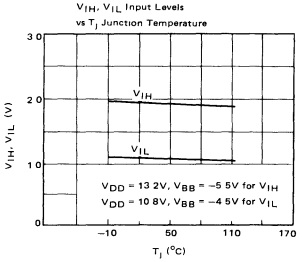

V_{IHC}, V_{ILC} Input Levels
vs V_{DD} Supply Voltage
V_{IHC}
V_{ILC}
V_{BB} = −5 5V for V_{IHC}
V_{BB} = −4 5V for V_{ILC}
T_j = 50°C
V_{IHC}, V_{ILC} (V)
3 0
2 0
1 0
0
8
10
12
14
16
V_{DD} (V)


V_{IH}, V_{IL} Input Levels
vs V_{DD} Supply Voltage
V_{IH}
V_{IL}
V_{BB} = −5 5V for V_{IH}
V_{BB} = −4 5V for V_{IL}
T_j = 50°C
V_{IH}, V_{IL} (V)
3 0
2 0
1 0
0
8
10
12
14
16
V_{DD} (V)


V_{IHC}, V_{ILC} Input Levels
vs V_{BB} Supply Voltage
V_{IHC}
V_{ILC}
V_{DD} = 13 2V for V_{IHC}
V_{DD} = 10 8V for V_{ILC}
T_j = 50°C
V_{IHC}, V_{ILC} (V)
3 0
2 0
1 0
0
−3
−4
−5
−6
−7
V_{BB} (V)


V_{IH}, V_{IL} Input Levels
vs V_{BB} Supply Voltage
V_{IH}
V_{IL}
V_{DD} = 13 2V for V_{IH}
V_{DD} = 10 8V for V_{IL}
T_j = 50°C
V_{IH}, V_{IL} (V)
3 0
2 0
1 0
0
−3
−4
−5
−6
−7
V_{BB} (V)

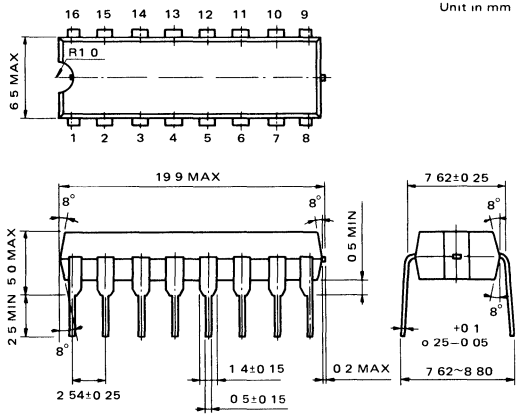

V_{IHC}, V_{ILC} Input Levels
vs T_j Junction Temperature
V_{IHC}
V_{ILC}
V_{DD} = 13 2V, V_{BB} = −5 5V for V_{IHC}
V_{DD} = 10 8V, V_{BB} = −4 5V for V_{ILC}
V_{IHC}, V_{ILC} (V)
3 0
2 0
1 0
0
−10
50
110
170
T_j (°C)


V_{IH}, V_{IL} Input Levels
vs T_j Junction Temperature
V_{IH}
V_{IL}
V_{DD} = 13 2V, V_{BB} = −5 5V for V_{IH}
V_{DD} = 10 8V, V_{BB} = −4 5V for V_{IL}
V_{IH}, V_{IL} (V)
3 0
2 0
1 0
0
−10
50
110
170
T_j (°C)

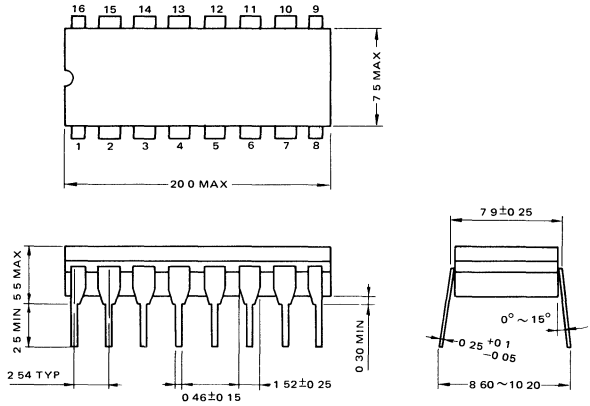
OUTLINE DRAWINGS

- **Plastic Package**

Unit in mm



- **Cerdip Package**



Note 1 Each lead pitch is 2 54mm All leads are located within 0 25mm of their true longitudinal position with respect to No 1 and No 16 leads
2 All dimensions are in millimeters

Note Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.