SECAM DECODER

GENERAL DESCRIPTION

The TDA4532 is a monolithic integrated colour decoder for SECAM television receivers. It is pin compatible with the multi-standard decoder TDA4555.

Features

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with rectifier which is disabled during horizontal and vertical flyback
- Chrominance output stage for driving the 64 μs glass delay line
- Limiter stages for direct and delayed chrominance signal
- SECAM permutator

Identification part

- Identification demodulator which is active during the horizontal identification signal and/or during part of the vertical flyback
- Identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Service switch for forced colour on
- Sandcastle pulse for detection of burst gating pulse, horizontal blanking pulse, combined horizontal and vertical blanking pulse. The vertical part of the sandcastle pulse is required for the internal colour ON and colour OFF delay
- Pulse processor part which prevents premature switch-on of the colour. A counter provides colour ON delay of 2 or 3 vertical periods after identification of the SECAM signal. Colour is switched off immediately the identification voltage disappears, or 1 vertical period later

Demodulator part

- Two quadrature demodulators with external reference tuned circuits
- Internal filtering of residual carrier in the demodulated colour difference signals
- De-emphasis circuit and colour switching stages in front of the output stages. The colour switching stages are controlled by the pulse processing part
- (B-Y) and (R-Y) colour difference output stages are low resistance n-p-n emitter followers

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	60 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$	20 to 400	mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
−(R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V
−(B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	min.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

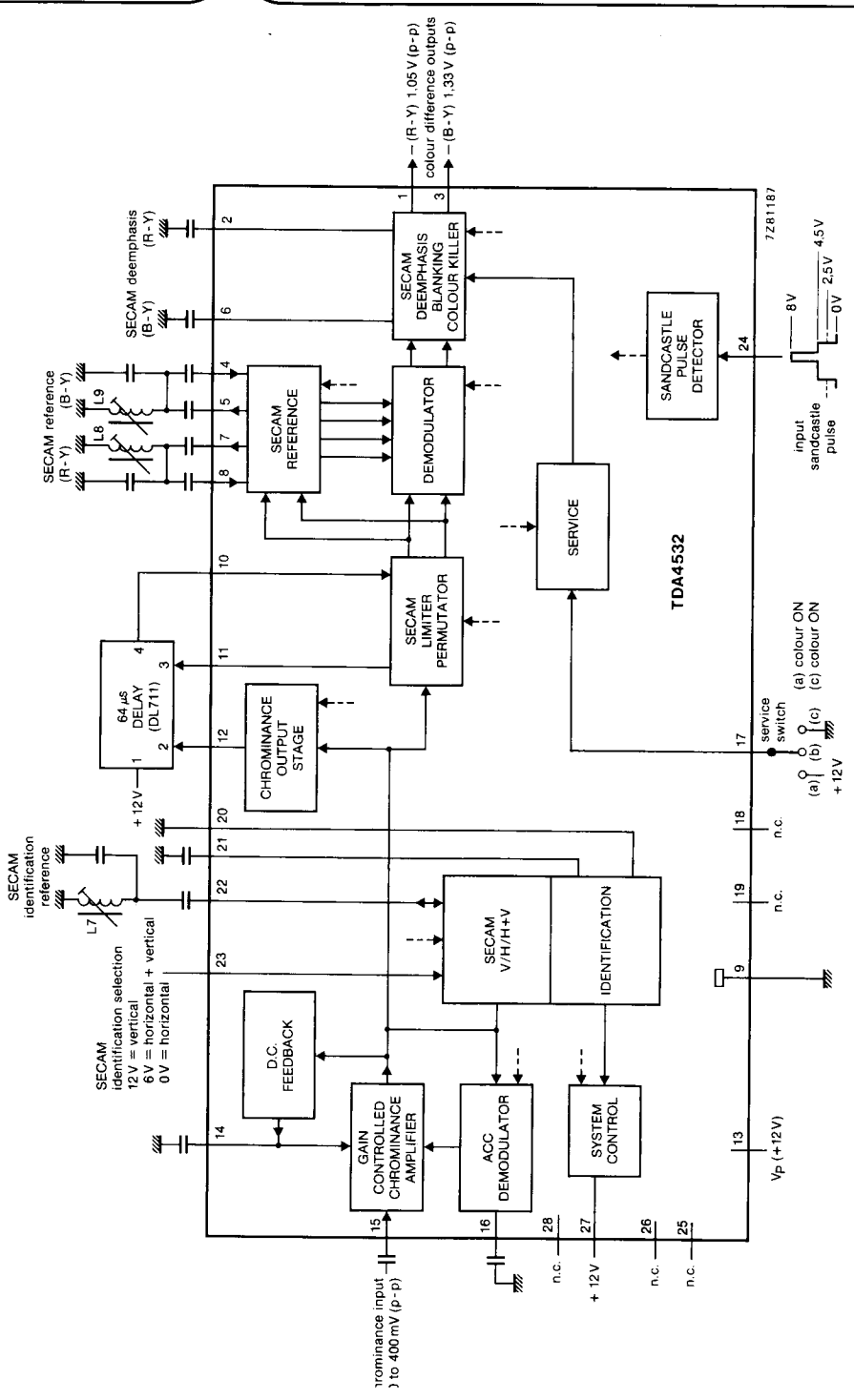

Fig. 1 Block diagram.

n.c. = not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 27 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	60	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	400	mV
input impedance	$\lvert Z_{15-9}\rvert$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12-9}\rvert$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part					
Colour difference output signals (note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
−(R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05*	–	V
−(B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33*	–	V
Ratio of colour difference output signals −(R-Y)/−(B-Y)	$V_{1/3-9}$	0,71*	0,79*	0,87*	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,\,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,\,3-9(p-p)}$	–	20	30	mV
H/2 ripple at −(R-Y) −(B-Y) outputs (peak-to-peak value) with f_o signals	$V_{1,\,3-9(p-p)}$	–	–	30	mV
D.C. output voltage	$V_{1,\,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only) with temperature	$\Delta V/\Delta T$	–	0,5*	0,6*	mV/K
with supply voltage	$\Delta V/\Delta V_P$	–	8,0*	15*	mV/K

* Value measured without influence of external circuitry.

parameter	symbol	min.	typ.	max.	unit
Identification mode switch (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6**	–	V
Colour killer delay time					
colour ON	t_{dC1}	–	–	3	field periods
colour OFF	t_{dC2}	–	–	1	field periods
Service switch					
Switching voltage (pin 17) (for forced colour ON)					
connected to ground	V_{17-9}	–	–	0,5	V
connected to supply voltage	V_{17-9}	6	–	–	V
Sandcastle pulse detector (note 2)					
Input voltage pulse levels (pin 24)					
to separate vertical and horizontal blanking pulses	V_{24-9}	1,3	1,6	1,9	V
required pulse amplitude	V_{24-9}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{24-9}	3,3	3,6	3,9	V
required pulse amplitude	V_{24-9}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{24-9}	6,6	7,1	7,6	V
required pulse amplitude	V_{24-9}	7,7	–	–	V
Input voltage during horizontal scanning	V_{24-9}	–	–	1,1	V
Input current	$-I_{24}$	–	–	100	μA

DEVELOPMENT DATA

Notes to the characteristics

1. The signal amplitude of the colour difference output signals −(R-Y) and −(B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

** Or not connected.

APPLICATION INFORMATION

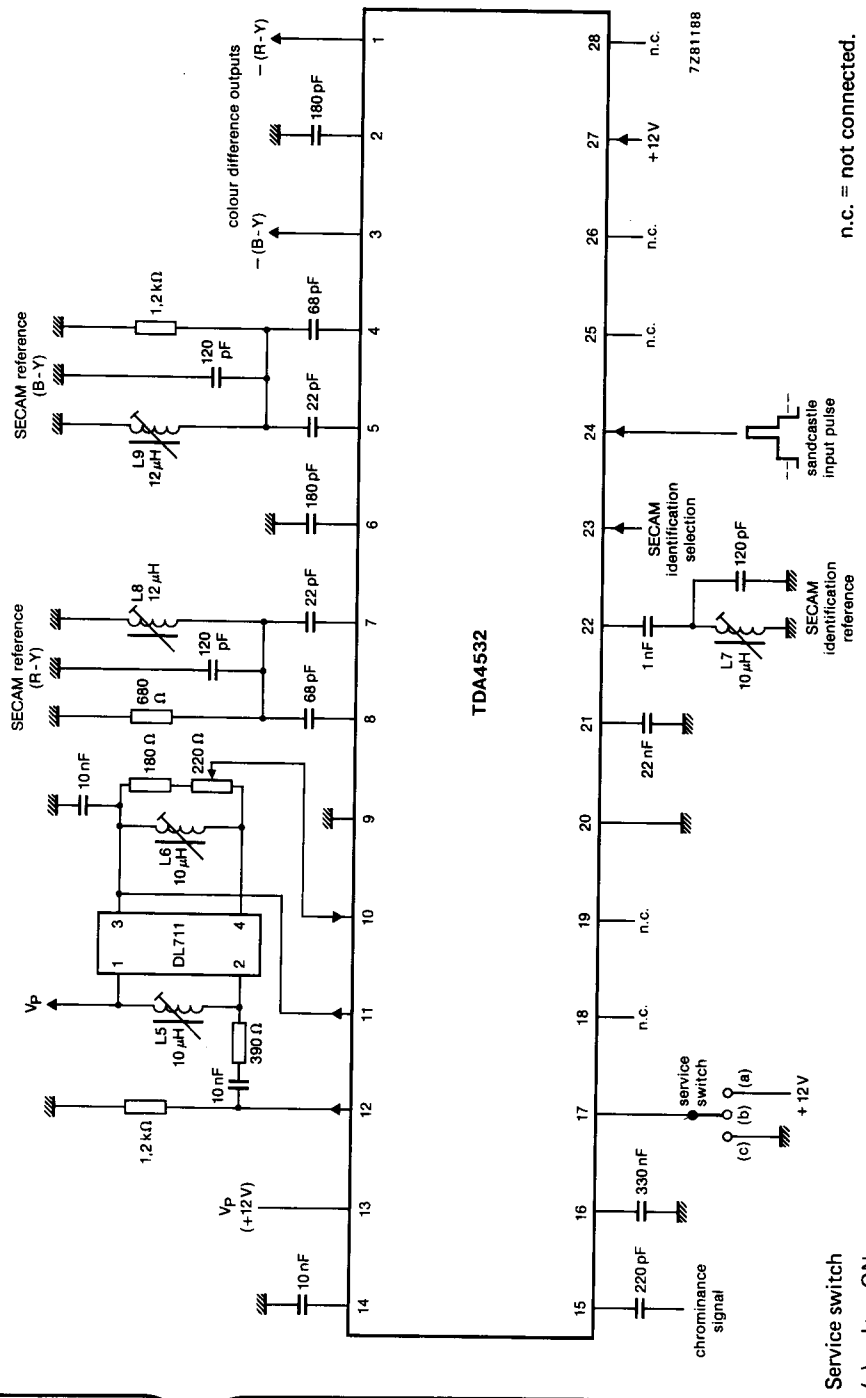

Fig. 2 Application diagram.

Service switch
(a) colour ON
(c) colour ON)