Signetics

TDA1534
14-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA1534 is a complete monolithic 14-bit analog-to-digital converter (ADC) which uses the successive approximation conversion technique and includes a 14-bit DAC, SAR, comparator, reference source, and clock on the chip. The digital functions are implemented with ECL logic with TTL level shifters interfacing with the device pins.

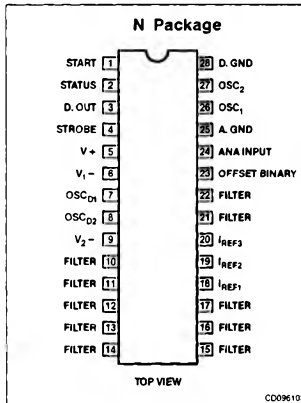
FEATURES

- **½ LSB linearity over temperature**
- **¼ LSB linearity at 25°C**
- **Accepts unipolar or bipolar signals**
- **TTL compatible logic lines**
- **Internal clock**
- **Internal reference**
- **High signal-to-noise ratio (84dB typ)**

APPLICATIONS

- **Automotive**
- **Digital audio**
- **Digital signal processing**
- **Instrumentation**
- **Medical electronics**
- **Industrial**

PIN CONFIGURATION

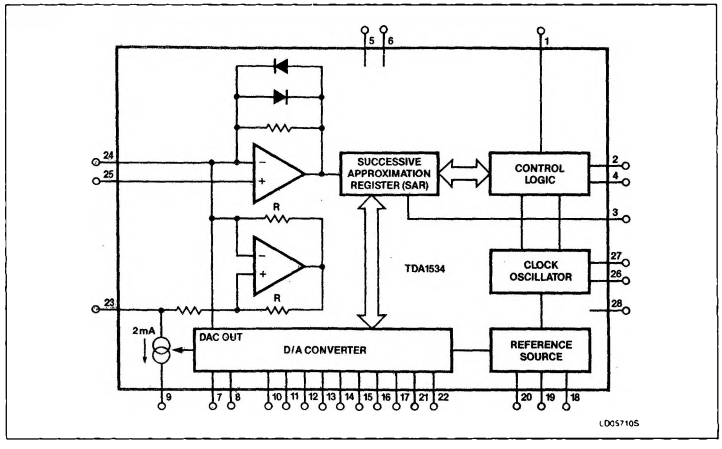


PIN NO.	DESCRIPTION
1	Start Conversion
2	Status Out
3	Data Out
4	Data Strobe
5	Positive Supply Voltage
6	Negative Supply Voltage 1
7	Oscillator Input
8	Oscillator Input
9	Negative Supply Voltage 2
10, 11, 12, 13, 14, 15, 16, 17	Filter
18	I_{REF1}
19	I_{REF2}
20	I_{REF3}
21, 22	Filter
23	Offset Binary Input
24	Analog Signal Input
25	Analog Ground
26	Oscillator
27	Oscillator
28	Digital Ground

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
Plastic 28-Pin DIP	–20°C to +70°C	TDA1534N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_+	Positive supply voltage (Pin 5)	7	V
V_1-	Negative supply voltage (Pin 6)	−7	V
V_2-	Negative supply voltage (Pin 6)	−20	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
P_D	Power dissipation (25°C)	3.5	W

DC ELECTRICAL CHARACTERISTICS

$V+ = 5V$, $V_1- = -5V$, $V_2- = -17V$, $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution			14		bits
ϵ_L	Linearity	−20°C to +70°C		± 1/4 ± 1/2		LSB LSB
I_{FS}	Full-scale analog input current	Pin 23 shorted to ground	3.8	4.0	4.2	mA
TC_A	Tempco of analog input current	Pin 23 shorted to ground		± 30		ppm/°C
V_O	Zero-scale offset voltage	Pin 23 shorted to ground	10	2 0	30	mV
TC_{VO}	Tempco of zero-scale offset voltage	0 to 50°C, Pin 23 grounded		80		µV/°C
I_{OS}	Zero-scale offset current	Pin 23 shorted to ground		500		nA
TC_{IO}	Tempco of input offset current	Pin 23 shorted to ground		1.5		nA/°C
I_{BO}	Offset binary current		0.45	0.50	0.55	I_{FS}
TC_{IBO}	Tempco of offset binary current			30		10^{-6}/°C
I_{IL}	Start conversion input current (Pin 1)	$V_{IL} < 0.8V$			−1.6	mA
I_{IH}	Start conversion input current (Pin 1)	$V_{IL} > 2.0V$			40	µA
I_{OL}	Output low current (Pins 2, 3, 4)	$V_{OL} < 0.6V$	6.4	16		mA
I_{OH}	Output high current (Pins 2, 3, 4)	$V_{OH} > 2.4V$	160	400		µA
S/N	Signal-to-noise ratio[1]		80	84		dB
V+	Positive supply voltage (Pin 5)		4	5	6	V
V_1-	Negative supply voltage (Pin 6)			−5		V
V_2-	Negative supply voltage (Pin 9)		−16.5	−17	−18	V
$I_{CC}+$	Positive supply current			30	40	mA
I_{CC-1}	Negative supply current			−37	−45	mA
I_{CC-2}	Negative supply current			−10	−13	mA
P_D	Power dissipation			500		mW

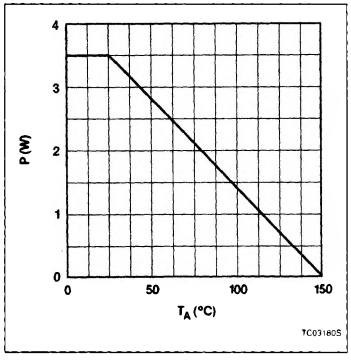
AC ELECTRICAL CHARACTERISTICS

$V+ = 5V$, $V_1- = -5V$, $V_2- = -17V$, $T_A = +25°C$, unless otherwise specified.

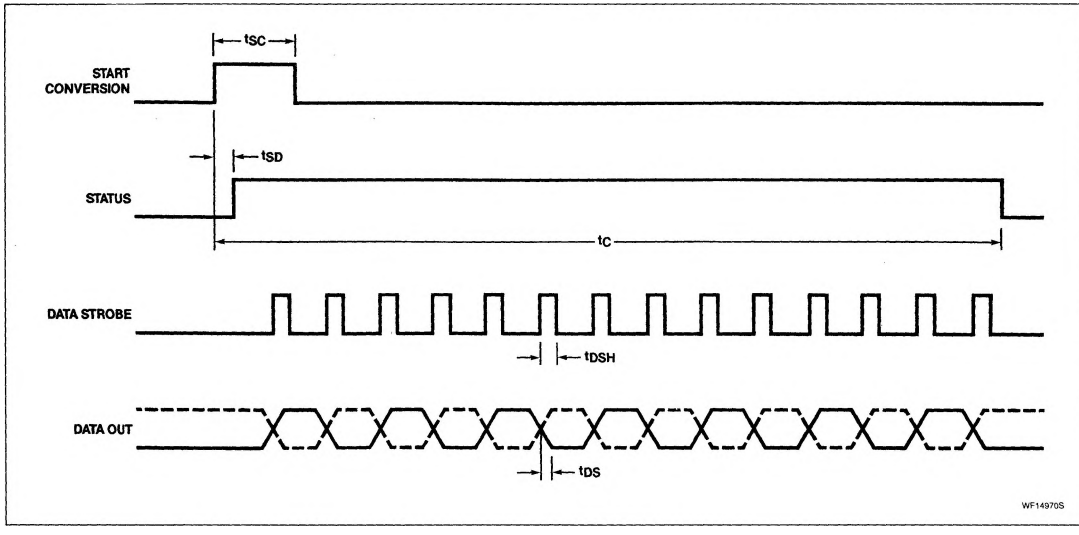
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{CONV}	Conversion time	Clock capacitor = 220pF Pins 26 – 27 (± 1%)		8.5		µs
t_{SC}	Start conversion pulse width	(Pin 1)	0.2			µs
t_{SD}	STATUS out delay time	(Pin 2)		60		ns
t_{DS}	DATA setup time	(Pin 3)		25		ns
t_{DSH}	DATA STROBE pulse duration	(Pin 4)		125		ns

NOTES:
Signal-to-noise ratio within 10Hz and 20kHz bandwidth of a 1kHz full-scale sinewave, generated at a sample rate of 44kHz.

POWER DERATING CURVE



SWITCHING TIME WAVEFORMS



FUNCTIONAL OPERATION AND USE

The TDA1534 Analog-to-Digital Converter (ADC) incorporates a 14-bit Digital-to-Analog Converter (DAC) that is functionally equivalent to the TDA1540 14-bit DAC. This DAC uses a unique **Dynamic Element Matching** scheme (Electronic Components and Applications, Vol. 2, No. 4, August 1980, by R.J. v. d. Plassche; IEEE Journal of Solid State Circuits, Vol. SC14, June 1979, pp. 552-556, by R.J. v. d. Plassche and D. Goedhardt) that insures 14-bit accuracy.

The Dynamic Element Matching technique requires an oscillator for current switching. In the TDA1534, the frequency of this oscillator is determined by the value of a capacitor between Pins 7 and 8. With the suggested 820pF capacitor, the internal clock frequency is about 160kHz. The capacitor value vs. oscillator frequency is a linear relationship. The conversion speed bears no relationship to this switching frequency because the switched currents are filtered and are simply DC values on the chip. The value of the ten filter capacitors is not particularly critical; −30% to +100% tolerance being allowed.

The acceptable frequency range for the Dynamic Element Marching oscillator is 150kHz to 250kHz. The minimum value arises from the fact that the divide-by-four action of the Dynamic Element Matching operation makes too low a frequency fall into the audio passband. The maximum value is needed because at high frequencies the oscillator jitter becomes too great a part of the clock period and causes inaccuracy in the Dynamic Element Matching current division and a loss of accuracy. It is suggested that the oscillator frequency be chosen so that it is close to the 150kHz minimum to keep the jitter from approaching ½ clock period. This would provide greatest accuracy.

The **Dynamic Element Matching** scheme takes each bit current and divides it in four. Two of these currents are combined to produce the current of the next lower bit. To insure that this current is half of its next higher bit, the two currents that are summed are sequenced in a predetermined pattern. For example, if the currents A, B, C, and D, we might first combine currents A and C, then A and D, then B and D, then A and B, etc., to allow for any small differences between individual currents, making the average current exactly half that of the next higher bit. In this way, high accuracy is obtained with high yield and relatively low cost. The disadvantage here is the requirement for the ten filter (decoupling) capacitors and the relatively large negative supply of 17V (use of 18V is quite permissible).

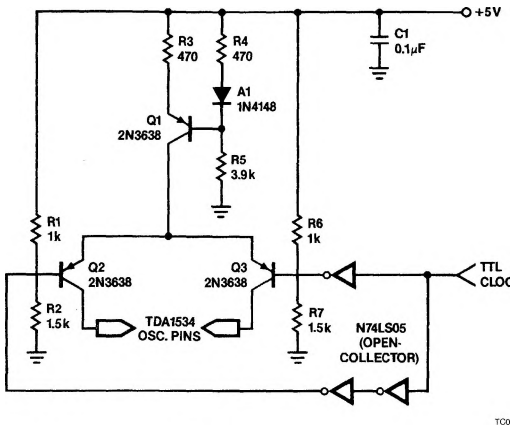


Figure 1. An Example of a Dual Current Source That may be Used to Drive the Oscillator Pins When an External Oscillator is Required. Note That Timing and the Number of Clock Cycles are Very Important for Proper Operation

The **Reference Source** is a temperature-corrected bandgap type. The 162Ω resistor at Pin 19 trims the bandgap PTC (positive temperature coefficient), while the 1200Ω resistor at Pin 20 is used to temperature-correct the reference with an NTC (negative temperature coefficient) that essentially cancels out the effect of the PTC, yielding a reference voltage that is constant over temperature. The 3.3nF (0.003μF) capacitor at Pin 18 is used for stabilizing the reference and offers a little noise filtering. It should be noted, however, that it is not reasonable to increase this capacitor to achieve additional noise filtering as its primary function is for circuit stabilization and the 3.3nF value is needed for this.

The **Clock Oscillator** with timing capacitor at Pins 26 and 27 is the A/D clock, which operates at about 3.5MHz with a 220pF capacitor between these two pins. The relationship between oscillator frequency and capacitance is linear, but a higher frequency (lower capacitance) will cause a loss of converter accuracy. A lower frequency (higher capacitance) will cause the conversion time to increase, although this will *not* result in an accuracy improvement. These pins can be driven in a complementary manner with two identical current sources if it is desired to use an external clock. See Figure 1 for a possible circuit to use with external clock drive. It is important that the Start Conversion signal begin within 10μs of the center of the time that the clock is at a logic low, that the clock have a 50% duty cycle, and that exactly 30 clock cycles occur during each conversion cycle. The converter requires 30 clock cycles for one conversion, yielding an 8.5μs conversion time at 3.5MHz clock frequency.

The **Status** output goes high to indicate a conversion in progress, and can be conveniently used to control a sample-and-hold amplifier such as the TDA1535. When the **Start Conversion** input (Pin 1) is brought high, the **Status** output immediately goes high, but there is a delay of two external clock periods (about ½μs) before conversion begins. The **Status** pin may, therefore, be connected to the Sample/Hold control pin of a Sample-and-Hold amplifier (as long as the input interprets a logic high to be a "Hold" signal), eliminating the need for two separate commands: one to the sample-and-hold amplifier and another to the A/D converter. See Figure 2.

Note that the TDA1535 acquisition time is stated at 2μs, yet conversion begins about ½μs after the Status output goes high. The acquisition time is the time it takes the sample-and-hold amplifier output to make a full range swing when going from sample (track) to hold. When the sample-and-hold is in the track or sample mode and goes to the hold mode, as is the case when the status output goes from a logic low to a logic high, the time for the sample-and-hold output to settle is much less, and the ½μs is sufficient time for the sample-and-hold amplifier to settle when going from the sample or track mode to the hold mode.

There are about 3 external clock periods (about 1.5 internal clock periods — the internal clock being half the frequency of the

external clock), or about 850ns, between the rise of the **Start Conversion** input to the fall of the first **Data Strobe** output, the center of the MSB data valid time.

The **Start Conversion** pulse must have a very fast rise time to insure that the **Status Output** goes high with minimum delay. With excessive delay in the **Status Output**, the sample-and-hold amplifier could go into the hold mode *after* the MSB is determined, adding inaccuracy to the conversion. Normal TTL switching speeds are adequate. Once a conversion has been started, the signal at the **Start Conversion** input will have no effect, so it is not possible to short cycle the TDA1534.

Data at the **Data Output** pin appears MSB (Most Significant Bit) first and the **Data Strobe** output pulses only appear while a conversion is in progress, going low each time a valid bit is present at the **Data Out** pin. Data should only be considered valid at the falling edge of this **Data Strobe** output, so a negative *edge-triggered* serial-in, parallel-out register should be used for serial-to-parallel conversion. Since shift register decoding is done within the TDA1534, there is no need to externally determine when the MSB is valid and when to stop clocking data into the shift register. The **Data Strobe** is used to directly load the shift register, simplifying circuit design. See Figure 2.

Pin 23 is the **Offset Binary** input pin. With this pin grounded, the converter will accept input currents in the range of 0 to 4mA. With a capacitor between Pin 23 and ground, the acceptable linear range of input currents is −2mA to +2mA, and the converter operates in the so-called "Offset Binary" mode. This pin should not be left floating as the converter accuracy could suffer due to energy from the Dynamic Element Matching oscillator feeding into the input, effectively adding 160kHz noise there.

The **Analog Signal Input**, Pin 24, is a virtual ground, so a series resistor is needed to limit the input current range to −2mA to +2mA with Pin 23 grounded through a capacitor, or to 0 to 4mA with Pin 23 at AC ground.

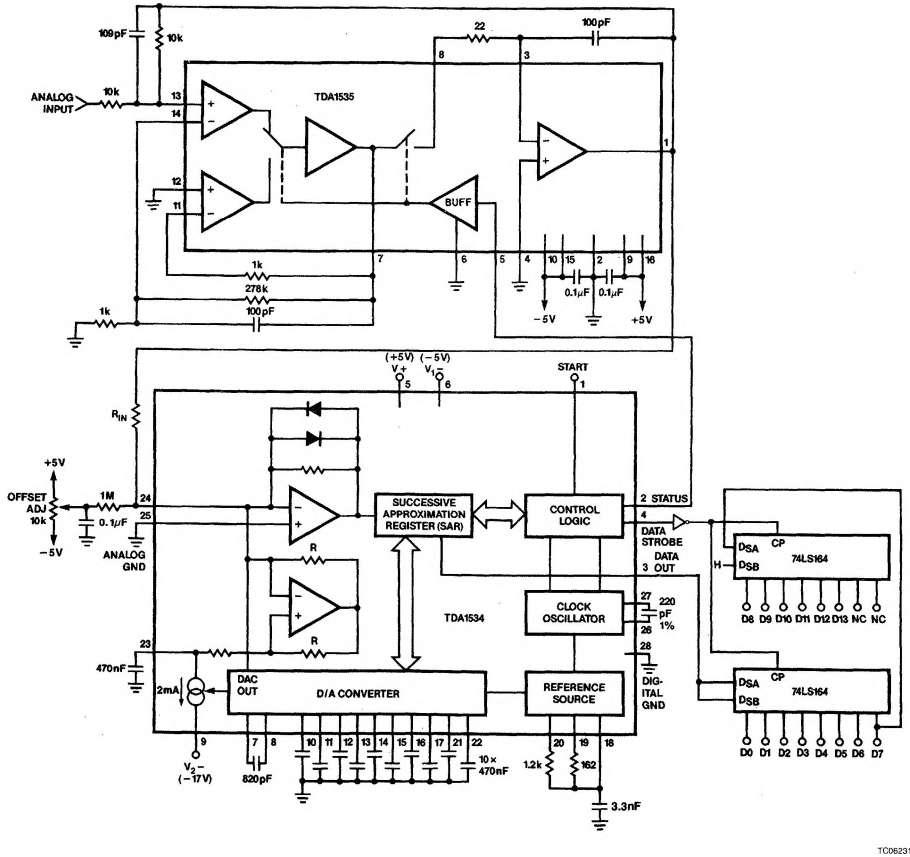


Figure 2. The Status Output Can Be Used to Control a Sample-and-Hold Amplifier, While the Data Strobe Output Controls a Serial-to-Parallel Shift Register

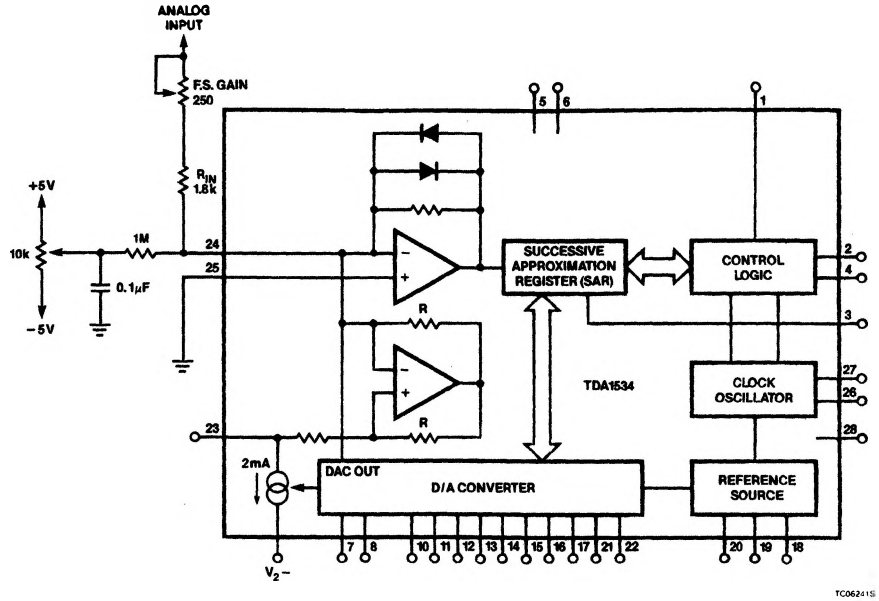


Figure 3. Zero-Scale Offset and Full-Scale Gain Adjustment

ZERO-SCALE OFFSET ADJUST

The analog signal input at Pin 24 is a current input and, to compensate for the zero-scale offset error, it is necessary to inject the proper current at Pin 24. This is easily accomplished by connecting the wiper of a potentiometer to Pin 24 in series with a 1MΩ resistor. Figure 3 illustrates how this may be accomplished.

FULL-SCALE GAIN ADJUSTMENT

Since the analog signal is a current input, the value of this current being determined by the analog voltage input and the value of the input resistor, R_{IN}, the Full-Scale Gain Adjustment, is simply making R_{IN} an adjustable resistor, or rheostat. The problem with a single adjustable resistor, however, is the fact that potentiometers have a rather large temperature coefficient. A gain adjustment that is reasonably stable would be a fixed film resistor in series with a rheostat, with the majority of the resistance in the fixed resistor. Figure 3 illustrates how this is accomplished.

AMBIENT TEMPERATURE CONSIDERATIONS

The TDA1534 is tested and rated for operation over the commercial temperature range (−20°C to +70°C). Above 70°C, the digital portion of the converter ceases to function and the converter will not operate at all. At temperatures much below −20°C the base-emitter junction voltage of the transistors increases to the point where the −17V supply is not sufficient to provide enough voltage to properly bias all the transistors that are stacked upon each other and accuracy begins to suffer. Increasing the negative supply to −19V *should* allow lower temperature operation, but behavior below −20°C is unknown and not guaranteed.

LAYOUT PRECAUTIONS

Layout of high bit count data converters requires a great deal of caution if maximum accuracy is to be realized. Just a little noise, as little as a few hundred microvolts, can cause errors as high as a few counts.

As is the case with all A/D converters, the analog ground and the digital ground must be connected together as close to the device as is possible. This is the only point on the board where the analog and digital grounds should be connected together. The signal return line should have its own path from the signal source return to the A/D converter analog ground to prevent ground noise fluctuations from detracting from converter accuracy. Neither the signal input line nor the signal return line should be run parallel to lines carrying digital information and should be as short as is reasonably possible.

As always with any linear IC, the power supplies should be as stable as possible and should be bypassed as close to the power supply pins as possible.

The oscillator should be located as close to the converter package as possible, as should the resistors and capacitor at Pins 18, 19, 20 and 23. The entire path from the input source to Pin 24 should be as short as possible, as should the trace from the STATUS output to the sample-and hold control input (if the STATUS output is used to control the sample-and-hold amplifier).