

TOSHIBA MOS MEMORY PRODUCTS

2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5517AP/-2, TC5517APL/-2
TC5517AD/-2, TC5517ADL/-2
TC5517AF/-2, TC5517AFL/-2

DESCRIPTION

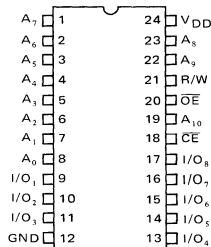
The TC5517AP/AD/AF is a 16384-bit static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5V supply.

The TC5517AP/AD/AF is featured by output enable and chip enable inputs, that is, $\overline{OE}$ for fast memory access and $\overline{CE}$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for non-

FEATURES

- Standby Current
 - 0.2 μ A (Max.) at $T_a = 25^\circ\text{C}$ } TC5517APL/
 - 1.0 μ A (Max.) at $T_a = 60^\circ\text{C}$ } ADL/AFL
 - 1.0 μ A (Max.) at $T_a = 25^\circ\text{C}$ } TC5517AP/
 - 5.0 μ A (Max.) at $T_a = 60^\circ\text{C}$ } AD/AF
- Low Power Dissipation : 200mW (Typ.) operating
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation

PIN CONNECTION (TOP VIEW)



PIN NAMES

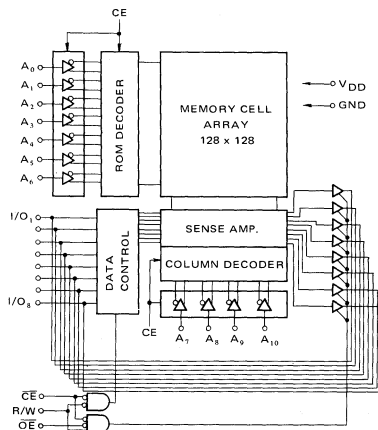
$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_0 \sim I/O_7$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

volatility are required. Furthermore the TC5517APL/ADL/AFL guaranteed a standby current equal to or less than 1 μ A at 60 $^\circ\text{C}$ ambient temperature is available.

The TC5517AP/AD is also featured by pin compatibility with 2716 type EPROM. This means that the TC5517AP/AD and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

- Access Time
 - 250ns (Max.) : TC5517AP/APL/AD/ADL/AF/AFL
 - 200ns (Max.) : TC5517AP-2/APL-2/AD-2/ADL-2/AF-2/AFL-2
- Two Control Input ($\overline{CE}$, $\overline{OE}$)
- Pin Compatible with Nch Static RAM TMM2016P
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
 - Plastic DIP : TC5517AP/APL
 - Cerdip DIP : TC5517AD/ADL
 - Plastic FP : TC5517AF/AFL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V_{IN}	Input Voltage	-0.3V ~ $V_{DD}+0.3V$
$V_{I/O}$	Input/Output Voltage	-0.3V ~ $V_{DD}+0.3V$
P_D	Power Dissipation ($T_a = 85^\circ\text{C}$)	0.8W (0.45W)*
T_{STG}	Storage Temperature	-55°C ~ 150°C
T_{OPR}	Operating Temperature	-30°C ~ 85°C
T_{SOLDER}	Soldering Temperature • Time	260°C • 10 sec.

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS ($T_a = -30^\circ\text{C} \sim 85^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D.C. CHARACTERISTICS ($T_a = -30^\circ\text{C} \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{DD}			—	—	±1.0	μA
I _{LO}	I/O Leakage Current	CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD}			—	—	±5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	-2.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			2.0	3.0	—	mA
I _{DDS1}	Standby Current	CE = 2.2V			—	1.0	3.0	mA
I _{DDS2}		CE = V _{DD} - 0.5V V _{DD} = 2 ~ 5.5V	TC5517APL/ ADL/AFL	Ta = 25°C	—	—	0.2	μA
				Ta = 60°C	—	—	1.0	
			TC5517AP/ AD/AF	Ta = 25°C	—	0.05	1.0	
				Ta = 60°C	—	—	5.0	
			Ta = 85°C	—	—	30		
I _{DDO1}	Operating Current	CE = 0V, V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0mA			—	40	70	mA
I _{DDO2}		CE = 0V, V _{IN} = V _{DD} /GND, I _{OUT} = 0mA			—	30	55	

Note : Typical values are at $T_a = 25^\circ\text{C}$, $V_{DD} = 5V$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
$C_{I/O}$	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)
• Read Cycle

SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AD-2/ADL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AD/ADL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	—	250	—	ns
t_{ACC}	Access Time	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	100	—	100	ns
t_{CO}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{COE}	$\overline{OE}$ or $\overline{CE}$ to Output Active	10	—	10	—	ns
t_{OD}	Output High-Z from Deselection	—	80	—	80	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	ns

• Write Cycle

SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AD-2/ADL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AD/ADL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	—	250	—	ns
t_{WP}	Write Pulse Width	160	—	200	—	ns
t_{AW}	Address Set Up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	ns
t_{ODW}	Output High-Z from R/W	—	80	—	80	ns
t_{OEW}	Output Active from R/W	10	—	10	—	ns
t_{DS}	Data Set Up Time	80	—	120	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

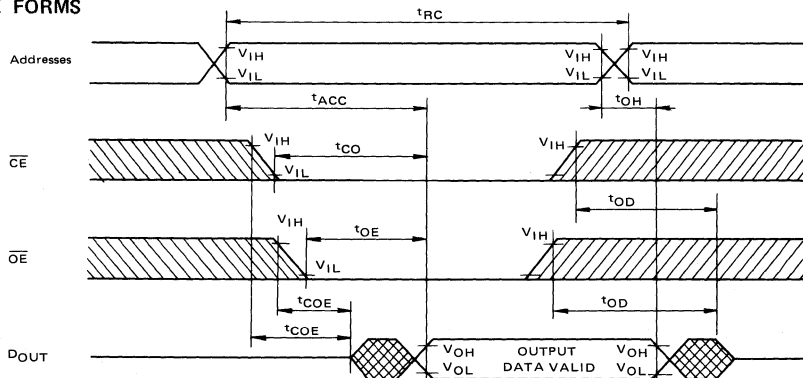
Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

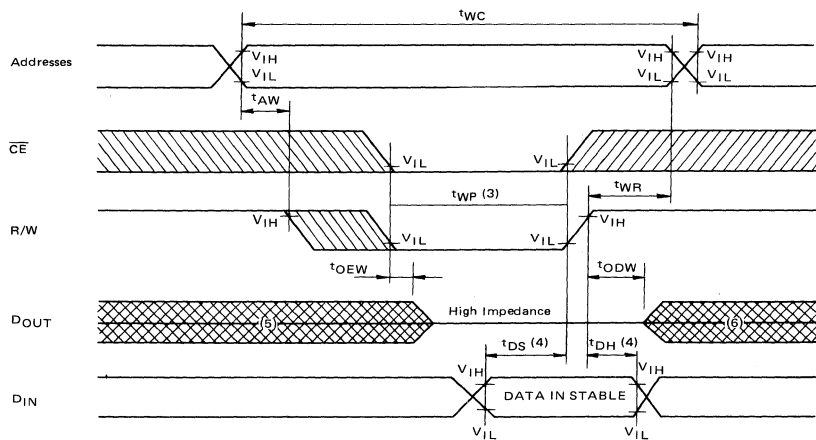
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

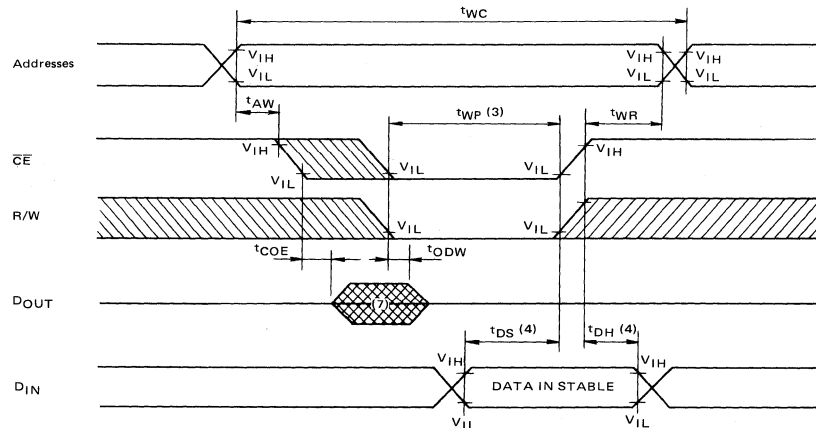
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS
• Read Cycle (1)


• Write Cycle 1 (1)



• Write Cycle 2 (2)



 : UNKNOWN

NOTE: (1) R/W is high for a Read Cycle.

(2) $\overline{OE} = V_{IH}$ or V_{IL} . If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.

(3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.

t_{WP} is measured from the latter of $\overline{CE}$ of R/W going low to the earlier of $\overline{CE}$ or R/W going high.

(4) t_{DH} , t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.

(5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

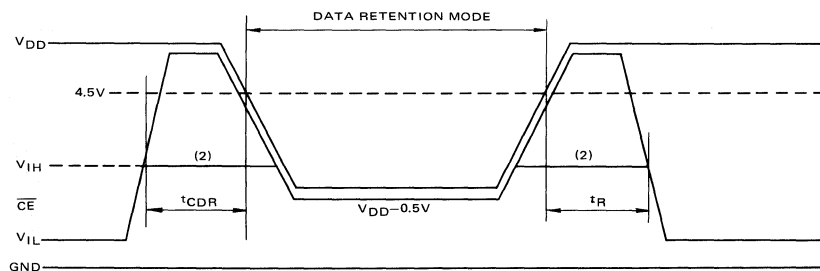
(6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage		2.0	—	5.5	V
I_{DD2}	Standby Current	TC5517APL/ ADL/AFL	$T_a = 25^\circ\text{C}$	—	0.2	μA
			$T_a = 60^\circ\text{C}$	—	1.0	
		TC5517AP/ AD/AF	$T_a = 25^\circ$	—	0.05	
			$T_a = 60^\circ\text{C}$	—	5.0	
			$T_a = 85^\circ\text{C}$	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		$t_{RC}(1)$	—	—	μs

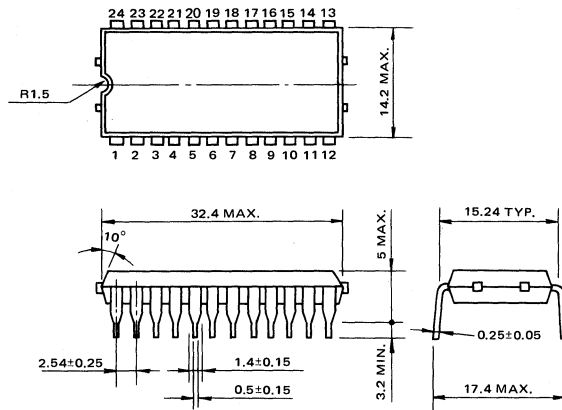
Note (1) t_{RC} : Read Cycle Time



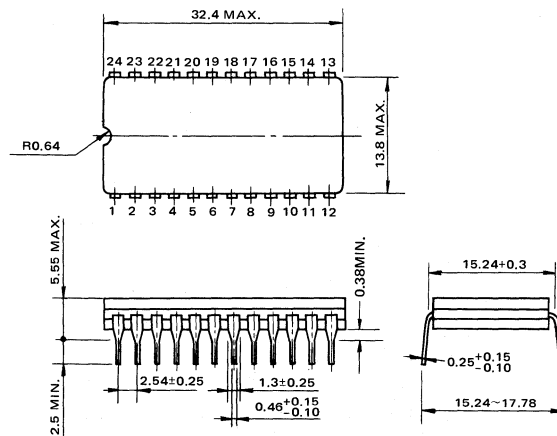
Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DD1} current flows.

OUTLINE DRAWINGS

• Plastic DIP



• Cerdip DIP



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.



PACKAGE INFORMATION FOR FLAT PACKAGE

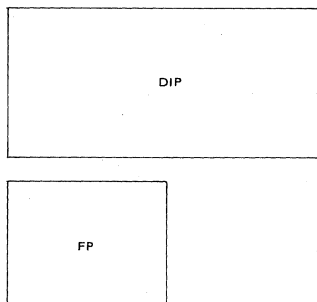
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit: mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

2. Comparison in occupied space



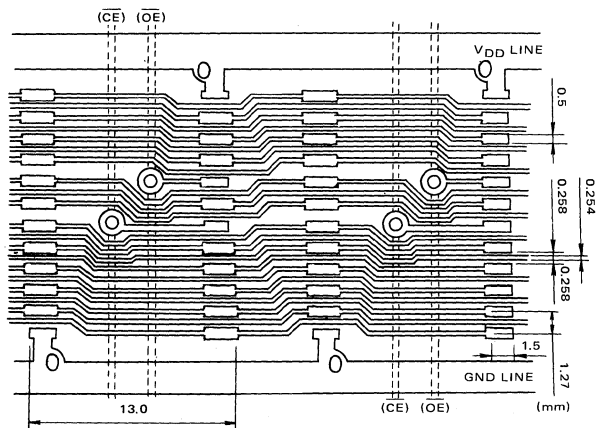
3. Advantage of this package

Small dimensions

Capability of High Density Assembly

Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

© Nov., 1981 Toshiba Corporation

OPERATION MODE

MODE	CE	OE	R/W	A ₀ ~ A ₁₀	I/O ₁ ~ ₈	POWER
Read	L	L	H	Stable	Data Out	I _{DDO}
Write	L	*	L	Stable	Data In	I _{DDO}
Output Deselect	*	H	*	*	High Impedance	I _{DDO}
**Standby	H	*	*	*	High Impedance	I _{DDS}

Note: *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V _{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V _{IN}	Input Voltage	-0.3V ~ V _{DD} + 0.3V
V _{I/O}	Input/Output Voltage	-0.3V ~ V _{DD} + 0.3V
P _D	Power Dissipation (Ta = 85°C)	0.8W (0.45W) *
T _{STG}	Storage Temperature	-55°C ~ 150°C
T _{OPR}	Operating Temperature	-30°C ~ 85°C
T _{SOLDER}	Soldering Temperature - Time	260 °C - 10 sec.

* Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = -30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V
V _{DH}	Data Retention Voltage	2.0	—	5.5	V

D.C. CHARACTERISTICS (Ta = -30°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT	
I _{IL}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{DD}		—	—	±1.0	μA	
I _{LO}	I/O Leakage Current	CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD}		—	—	±5.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4V		−1.0	−2.0	—	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4V		2.0	3.0	—	mA	
I _{DDs1}	Standby Current	CE = 2.2V		—	1.0	3.0	mA	
I _{DDs2}		CE ≥ V _{DD} −0.5V	TC5517BPL	Ta=25°C	—	—	0.2	μA
			/BDL/BFL-20	Ta=60°C	—	—	1.0	
		V _{DD} = 2 ~ 5.5V	TC5517BP/	Ta=25°C	—	0.05	1.0	
			BD/BF-20	Ta=60°C	—	—	5.0	
			Ta=85°C	—	—	30		
I _{DDO1}	Operating Current	t _{cycle} = 200ns	V _{IN} = V _{IH} /V _{IL}	—	—	30	mA	
I _{DDO2}		CE = 0V, I _{OUT} = 0mA	V _{IN} = V _{DD} /GND	—	—	25		
I _{DDO3}		t _{cycle} = 1μs	V _{IN} = V _{IH} /V _{IL}	—	—	10		
I _{DDO4}		CE = 0V, I _{OUT} = 0mA	V _{IN} = V _{DD} /GND	—	—	5		

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	—	5	10	pF
C _{I/O}	Input/Output Capacitance	—	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)
• Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{OE}	OE to Output Valid	—	70	ns
t_{CO}	$\overline{CE}$ to Output Valid	—	200	ns
t_{COE}	OE or $\overline{CE}$ to Output Active	10	—	ns
t_{OD}	Output High-Z from Deselection	—	60	ns
t_{OH}	Output Hold from Address Change	10	—	ns

• Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	—	ns
t_{WP}	Write Pulse Width	150	—	ns
t_{AW}	Address Set up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	Output High-Z from R/W	—	60	ns
t_{OEW}	Output Active from R/W	10	—	ns
t_{DS}	Data Set up time	90	—	ns
t_{DH}	Data Hold Time	0	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

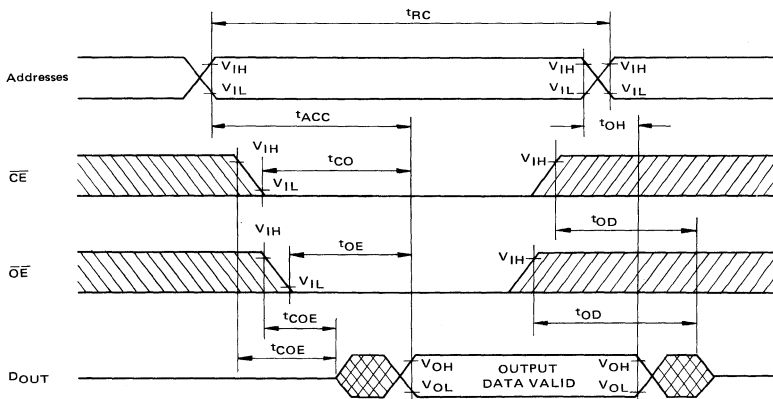
Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

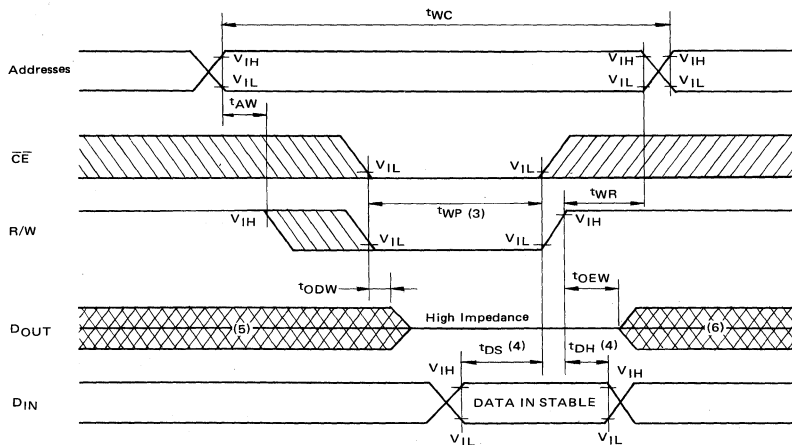
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

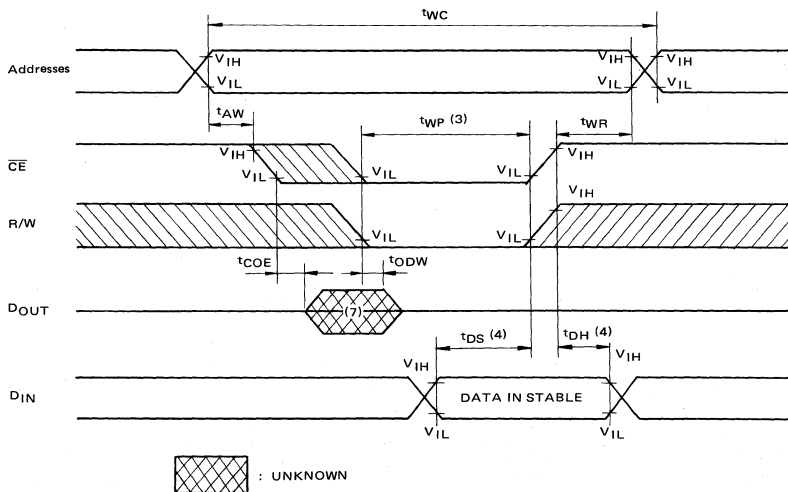
Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS
• Read Cycle (1)


• Write Cycle 1 (2)



• Write Cycle 2 (2)

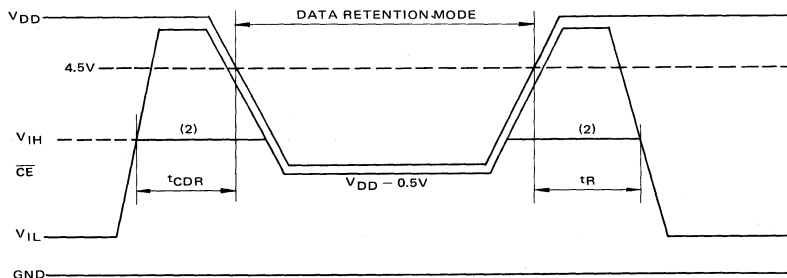


- Note: (1) R/W is high for a Read Cycle.
 (2) $\overline{OE} = V_{IH}$ or V_{IL} . If, $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
 (3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.
 t_{WP} is measured from the latter of $\overline{CE}$ or R/W going low to the earlier of $\overline{CE}$ or R/W going high.
 (4) t_{DH} , t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.
 (5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage		2.0	—	5.5	V
I_{DPS2}	Standby Current	TC5517BPL/ BDL/BFL-20	$T_a=25^\circ\text{C}$	—	0.2	μA
			$T_a=60^\circ\text{C}$	—	1.0	
		TC5517BP/ BD/BF-20	$T_a=25^\circ\text{C}$	0.05	1.0	
			$T_a=60^\circ\text{C}$	—	5.0	
			$T_a=85^\circ\text{C}$	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		$t_{RC}(1)$	—	—	μs

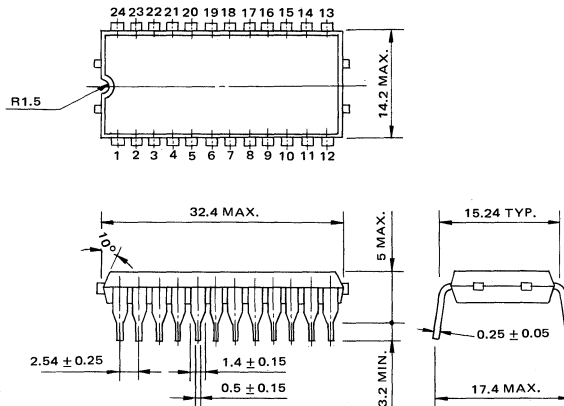
Note (1) t_{RC} : Read Cycle Time



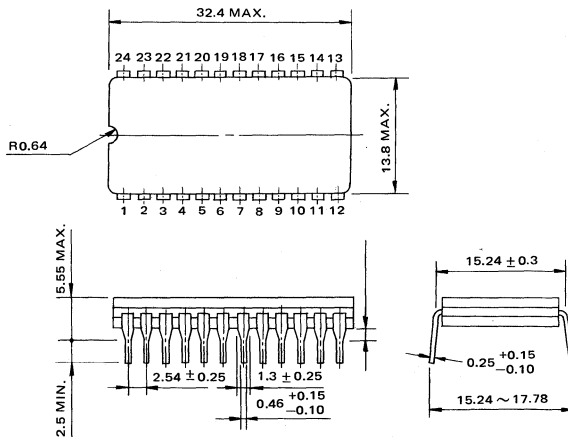
Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DPS1} current flows.

OUTLINE DRAWINGS

● Plastic DIP

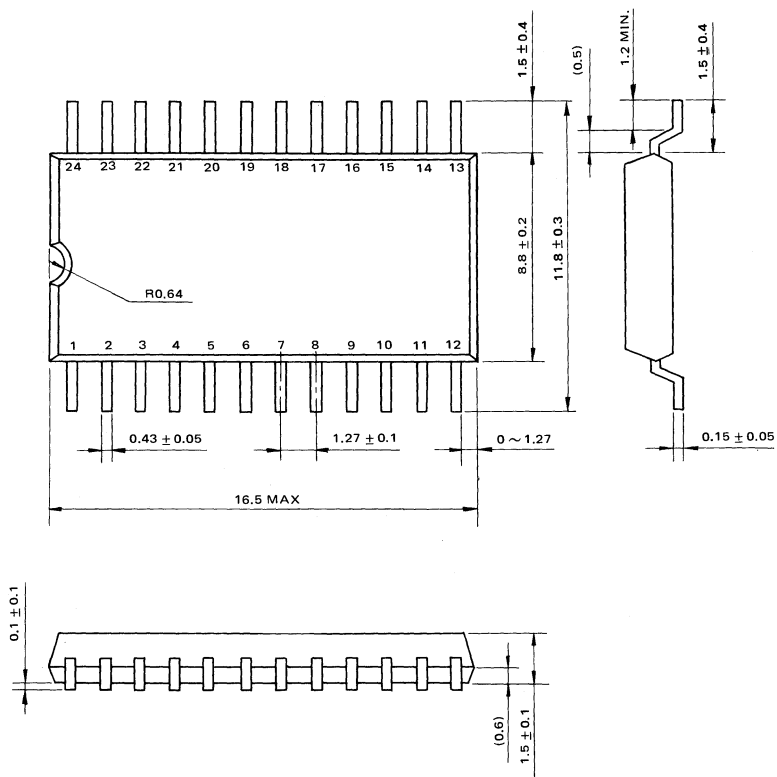


● Cerdip DIP



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

● Plastic FP



Note: Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

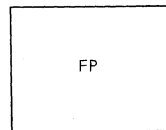
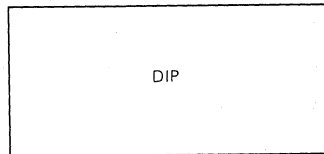
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit :mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

2. Comparison in occupied space



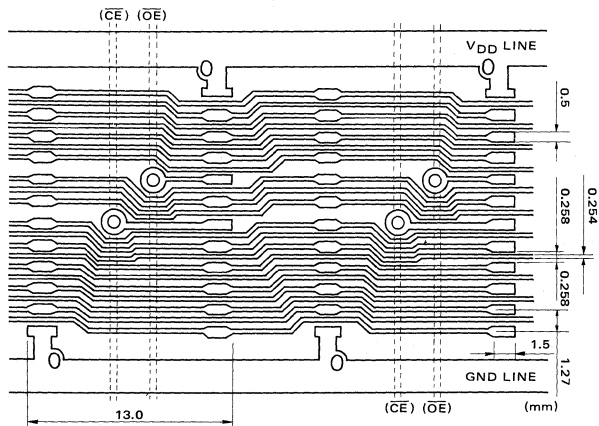
3. Advantage of this package

Small dimensions

Capability of High Density Assembly

Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

© Mar., 1983 Toshiba Corporation