

TOSHIBA MOS MEMORY PRODUCTS

2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5516AP/-2, TC5516APL/-2
TC5516AD/-2, TC5516ADL/-2
TC5516AF/-2, TC5516AFL/-2

DESCRIPTION

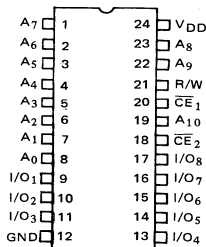
The TC5516AP/AD/AF is a 16384-bit static random access memory organized as 2048 words by 8 bit using CMOS technology, and operates from a single 5 volt supply.

The TC5516AP/AD/AF is featured by two chip enable inputs, that is, $\overline{CE}_1$ for fast memory access and $\overline{CE}_2$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5516APL/ADL/AFL

FEATURES

- Standby Current
 - $0.2\mu A$ (Max.) at $T_a = 25^\circ C$ } TC5516APL/
 - $1.0\mu A$ (Max.) at $T_a = 60^\circ C$ } ADL/AFL
 - $1.0\mu A$ (Max.) at $T_a = 25^\circ C$ } TC5516AP/
 - $5.0\mu A$ (Max.) at $T_a = 60^\circ C$ } AD/AF
- Low Power Dissipation : 200mW (Typ.) Operating
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation

PIN CONNECTION (TOP VIEW)



PIN NAMES

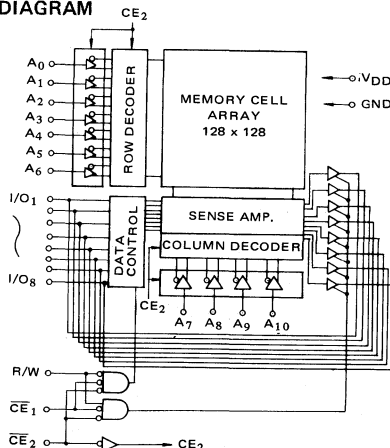
$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

guaranteed a standby current equal to or less than $1\mu A$ at $60^\circ C$ ambient temperature is available.

The TC5516AP/AD is also featured by pin compatibility with 2716 type EPROM. This means that the TC5516AP/AD and EPROM can be in terchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

- Access Time
 - 250ns (Max.): TC5516AP/APL/AD/ADL/AF/AFL
 - 200ns (Max.): TC5516AP-2/APL-2/AD-2/ADL-2 AF-2/AFL-2
- Two Chip Enable ($\overline{CE}_1, \overline{CE}_2$) for Simple Memory Expansion and Battery Back Up.
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
 - Plastic DIP : TC5516AP/APL
 - Cerdip DIP : TC5516AD/ADL
 - Plastic FP : TC5516AF/AFL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	$-0.3V \sim 7.0V$
V_{IN}	Input Voltage	$-0.3V \sim V_{DD} + 0.3$
$V_{I/O}$	Input/Output Voltage	$-0.3V \sim V_{DD} + 0.3$
P_D	Power Dissipation ($T_a = 85^\circ C$)	0.8W (0.45W) *
T_{STG}	Storage Temperature	$-55^\circ C \sim 150^\circ C$
T_{OPR}	Operating Temperature	$-30^\circ C \sim 85^\circ C$
T_{SOLDER}	Soldering Temperature · Time	$260^\circ C \cdot 10 \text{ sec}$

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS ($T_a = -30^\circ C \sim 85^\circ C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D.C. CHARACTERISTICS ($T_a = -30^\circ C \sim 85^\circ C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{DD}			—	—	±1.0	μA
I _{LO}	I/O Leakage Current	CE ₂ = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD}			—	—	±5.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V			-1.0	-2.0	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V			2.0	3.0	—	mA
I _{DDS1}	Standby Current	CE ₂ = 2.2V			—	1.0	3.0	mA
I _{DDS2}		CE ₂ = V _{DD} -0.5V	TC5516APL/ ADL/AFL	Ta = 25°C	—	—	0.2	μA
				Ta = 60°C	—	—	1.0	
		V _{DD} = 2 ~ 5.5V	TC5516AP/ AD/AF	Ta = 25°C	—	0.05	1.0	
				Ta = 60°C	—	—	5.0	
			Ta = 85°C	—	—	30		
I _{DDO1}	Operating Current	CE ₂ = 0V, V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0mA			—	40	70	mA
I _{DDO2}		CE ₂ = 0V, V _{IN} = V _{DD} /GND, I _{OUT} = 0mA			—	30	55	

Note: Typical values are at $T_a = 25^\circ C$, $V_{DD} = 5V$.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
$C_{I/O}$	Input/Output Capacitance	—	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = -30 ~ 85°C, VDD = 5V ± 10%)

• Read Cycle

SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AD-2/ADL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AD/ADL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	200	—	250	—	ns
t _{ACC}	Access Time	—	200	—	250	ns
t _{CO1}	$\overline{CE}_1$ to Output Valid	—	100	—	100	ns
t _{CO2}	$\overline{CE}_2$ to Output Valid	—	200	—	250	ns
t _{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	—	10	—	ns
t _{OD}	Output High-Z from Deselection	—	80	—	80	ns
t _{OH}	Output Hold from Address Change	10	—	10	—	ns

• Write Cycle

SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AD-2/ADL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AD/ADL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	200	—	250	—	ns
t _{WP}	Write Pulse Width	160	—	200	—	ns
t _{AW}	Address Set Up Time	0	—	0	—	ns
t _{WR}	Write Recovery Time	10	—	10	—	ns
t _{ODW}	Output High-Z from R/W	—	80	—	80	ns
t _{OE}	Output Active from R/W	10	—	10	—	ns
t _{DS}	Data Set Up Time	80	—	120	—	ns
t _{DH}	Data Hold Time	0	—	0	—	ns

A.C. TEST CONDITIONS

Output Load : 100 pF + ITTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

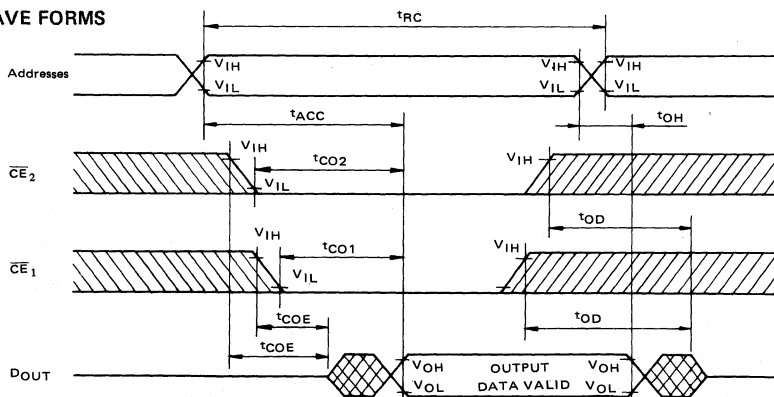
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

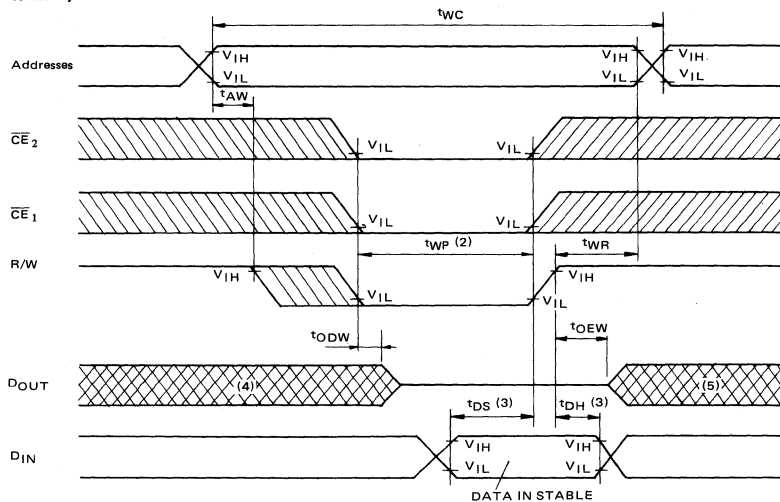
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS

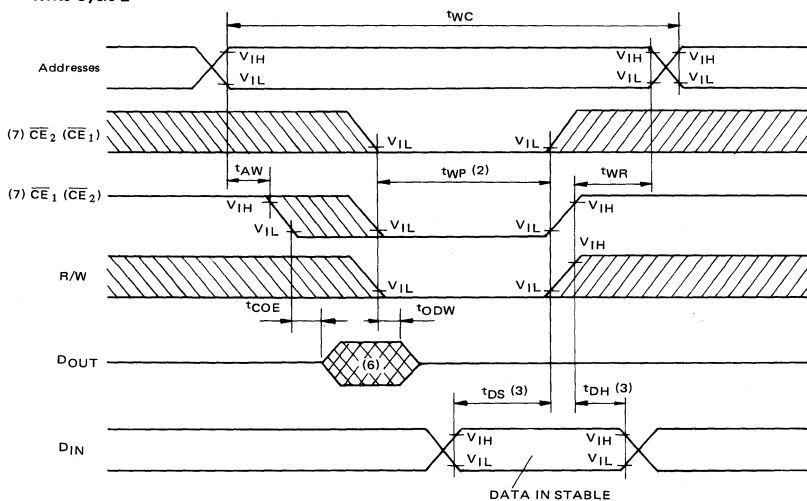
• Read Cycle



• Write Cycle 1



• Write Cycle 2



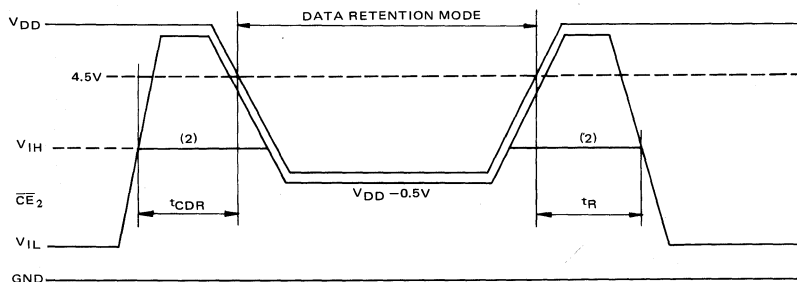
: UNKNOWN

- NOTE: (1) R/W is high for a Read Cycle.
- (2) t_{WP} is specified as the logical "AND" of $\overline{CE}_1$, $\overline{CE}_2$ and R/W.
 t_{WP} is measured from the latter of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going low to the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
- (3) t_{DH} , t_{DS} are measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
- (4) If the $\overline{CE}_1$, or $\overline{CE}_2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
- (5) If the $\overline{CE}_1$ or $\overline{CE}_2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
- (6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}_1$ or $\overline{CE}_2$ low transition, the output buffers remain in a high impedance state in this period.
- (7) A write occurs during the overlap of a low $\overline{CE}_1$, low $\overline{CE}_2$ and low R/W. In write cycle 2, write is controlled by either $\overline{CE}_1$ or $\overline{CE}_2$.

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

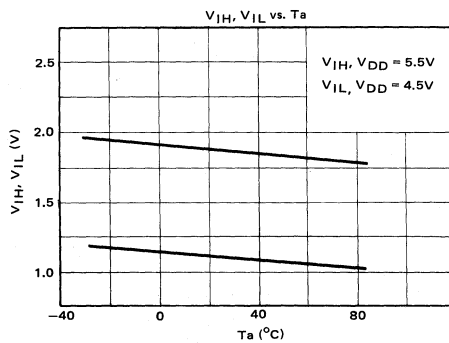
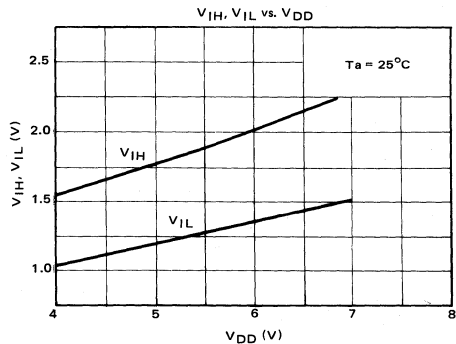
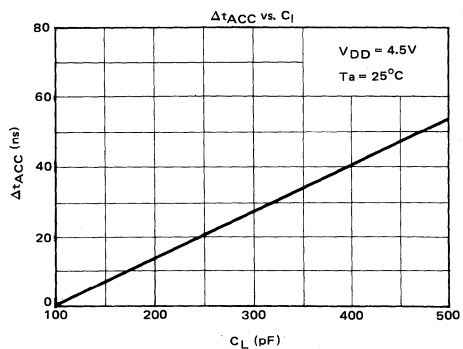
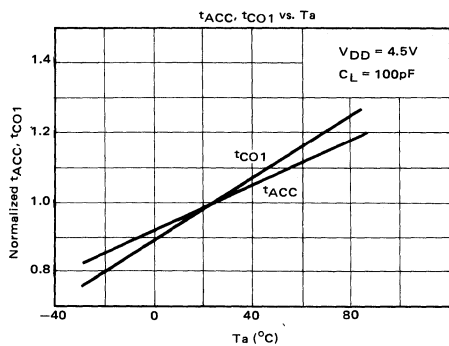
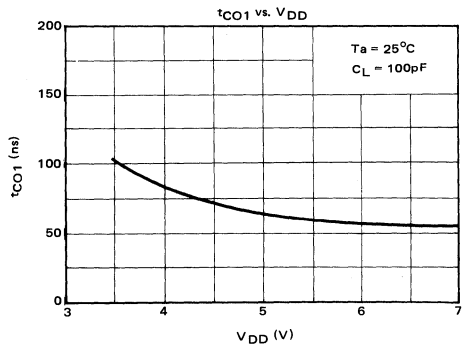
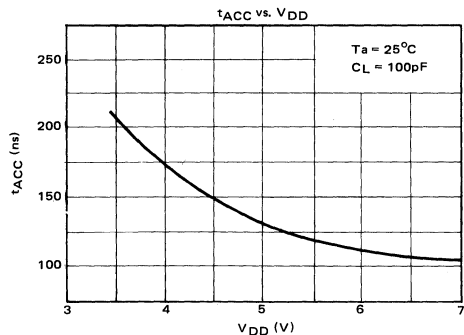
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage	2.0	—	5.5	V
I_{DDS}	Standby Current	TC5516APL/ ADL/AFL $T_a = 25^\circ\text{C}$	—	—	0.2
			—	—	1.0
		TC5516AP/ AD/AF $T_a = 25^\circ\text{C}$	—	0.05	1.0
			—	—	5.0
			—	—	30
t_{CDR}	From Chip Deselection to Data Retention Mode	0	—	—	μs
t_R	Recover Time	t_{RC} (1)	—	—	μs

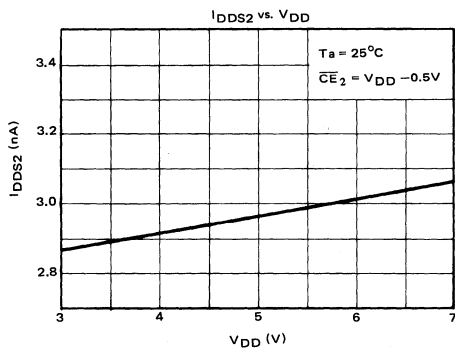
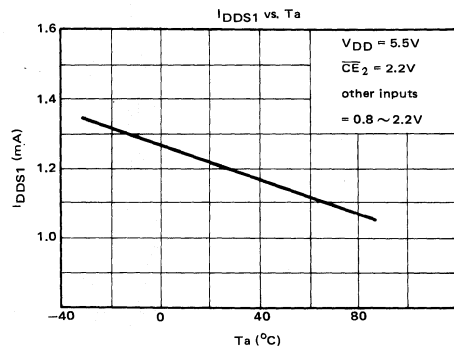
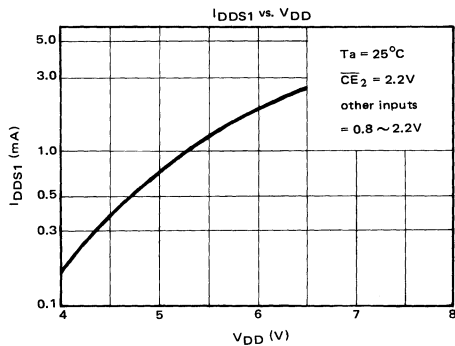
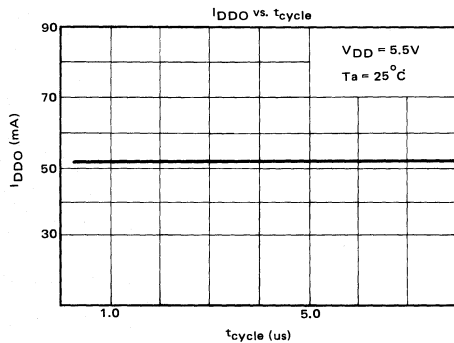
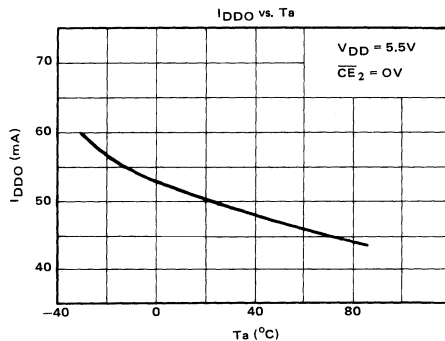
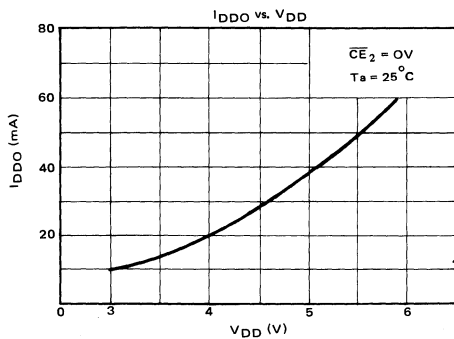
Note (1) t_{RC} : Read Cycle Time.

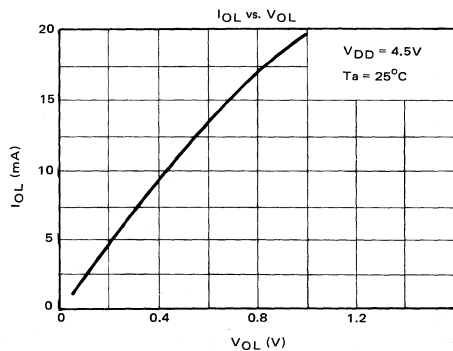
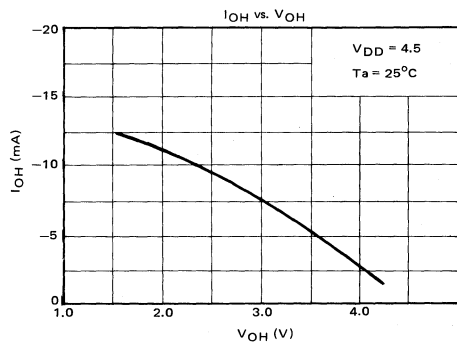
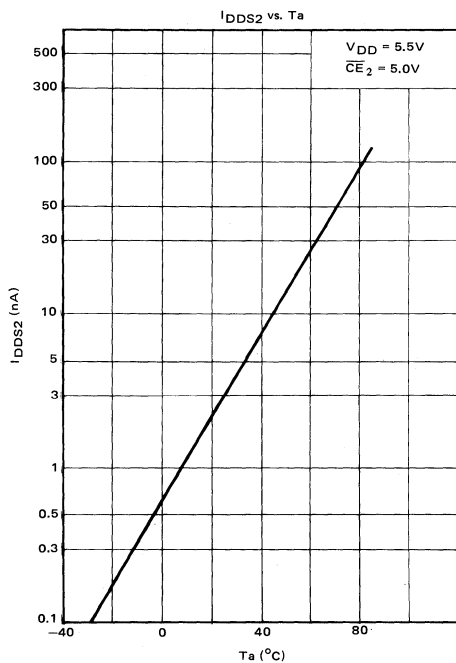
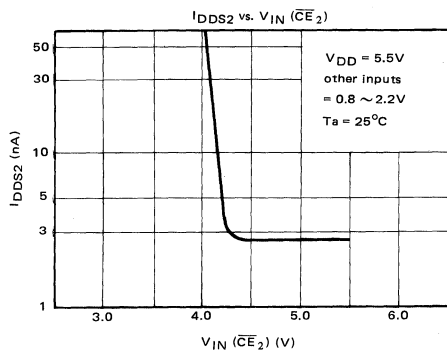
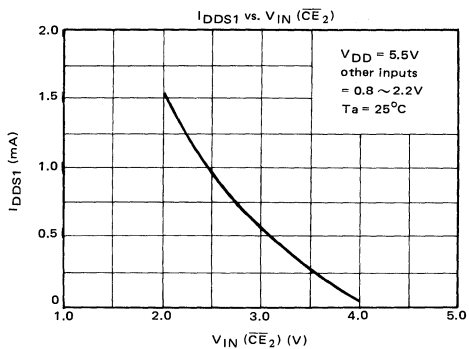


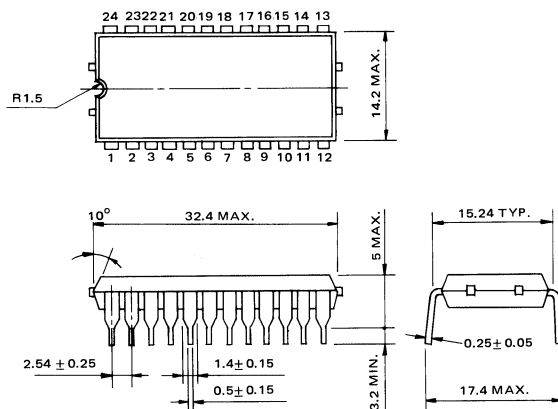
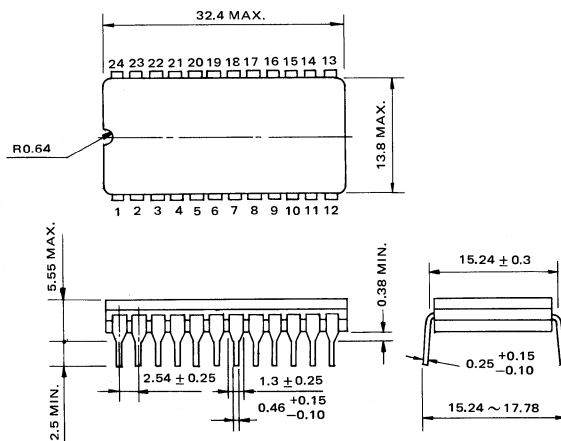
Note: (2) If the V_{IH} level of $\overline{CE}_2$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{SSD1} current flows. (Refer to D.C. CHARACTERISTICS or TYPICAL CHARACTERISTIC FIGURES.)

TYPICAL CHARACTERISTICS



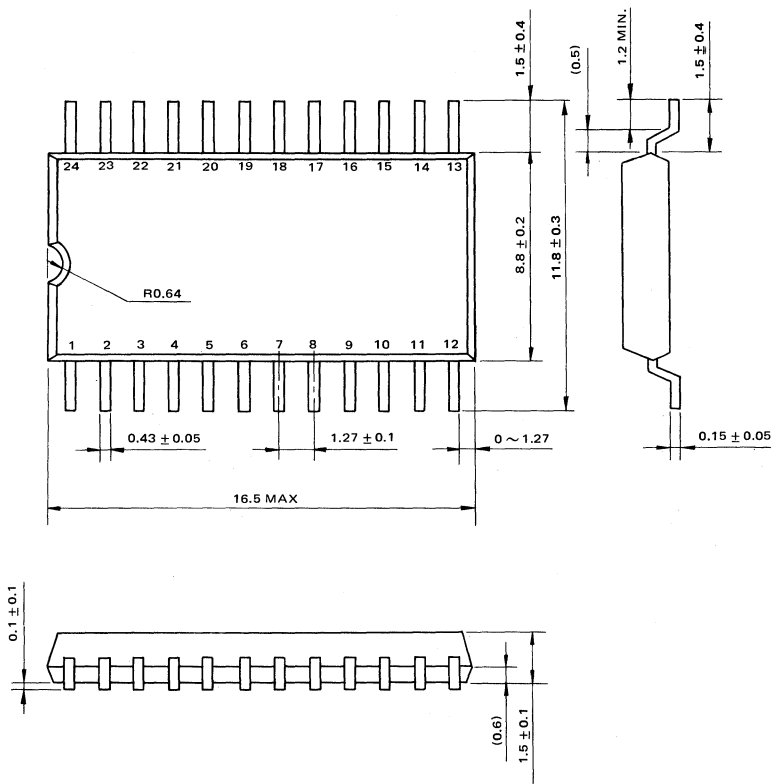




OUTLINE DRAWINGS
• Plastic DIP

• Cerdip DIP


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

● Plastic FP



Note: Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

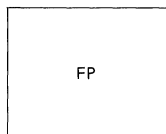
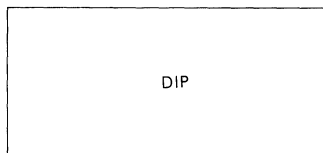
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

2. Comparison in occupied space.



3. Advantage of this package

- Small dimensions
- Capability of High Density Assembly
- Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example

