SN65176B, SN75176B
DIFFERENTIAL BUS TRANSCEIVERS

- **Bidirectional Transceivers**
- **Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operate From Single 5-V Supply**

SN65176B . . . D OR P PACKAGE
SN75176B . . . D, P, OR PS PACKAGE
(TOP VIEW)

R	1	8 V_{CC}
$\overline{RE}$	2	7 B
DE	3	6 A
D	4	5 GND
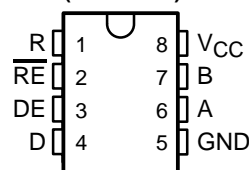
description/ordering information

The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	SN75176BP	SN75176BP
	SOIC (D)	Tube of 75	SN75176BD	75176B
		Reel of 2500	SN75176BDR	
	SOP (PS)	Reel of 2000	SN75176BPSR	A176B
−40°C to 105°C	PDIP (P)	Tube of 50	SN65176BP	SN65176BP
	SOIC (D)	Tube of 75	SN65176BD	65176B
		Reel of 2500	SN65176BDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.
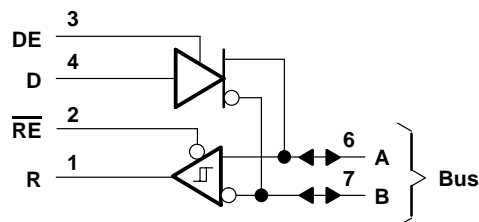
Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{\text{RE}}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT	TYPICAL OF A AND B I/O PORTS	TYPICAL OF RECEIVER OUTPUT

Driver input: $R_{(eq)}$ = 3 kΩ NOM
Enable inputs: $R_{(eq)}$ = 8 kΩ NOM
$R_{(eq)}$ = Equivalent Resistor
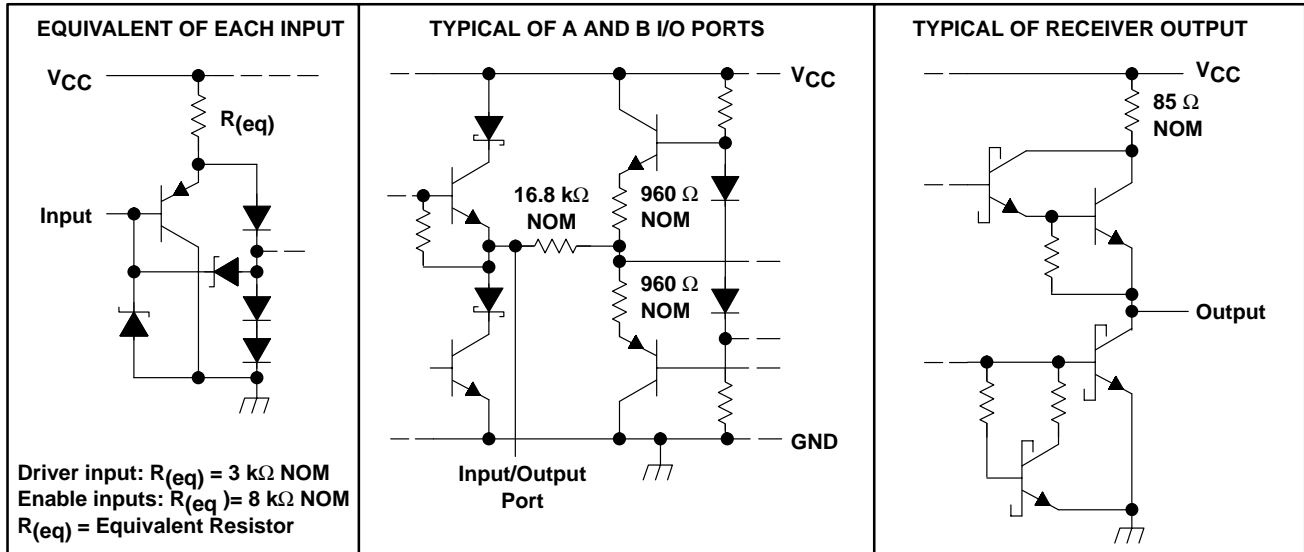
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1) .... 7 V
Voltage range at any bus terminal .... −10 V to 15 V
Enable input voltage, V_I .... 5.5 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package .... 97°C/W
                        P package .... 85°C/W
                        PS package .... 95°C/W
Operating virtual junction temperature, T_J .... 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					−7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage (see Note 4)				±12	V
I_{OH}	High-level output current	Driver			−60	mA
		Receiver			−400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65176B	−40		105	°C
		SN75176B	0		70	

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal A, with respect to the inverting terminal B.

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5	3.6	6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100$ Ω, See Figure 1		1/2 V_{OD1} or 2¶			V
		$R_L = 54$ Ω, See Figure 1		1.5	2.5	5	
V_{OD3}	Differential output voltage	See Note 5		1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage§	$R_L = 54$ Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54$ Ω or 100 Ω, See Figure 1				+3 −1	V
$\Delta|V_{OC}|$	Change in magnitude of common-modeoutput voltage§	$R_L = 54$ Ω or 100 Ω, See Figure 1				±0.2	V
I_O	Output current	Output disabled, See Note 6	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTES: 5. See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
6. This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics, $V_{CC} = 5$ V, $R_L = 110$ Ω, $T_A = 25°C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54$ Ω, See Figure 3			15	22	ns
$t_{t(OD)}$	Differential-output transition time	$R_L = 54$ Ω, See Figure 3			20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4			85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5			40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4			150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5			20	30	ns

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SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$|V_{OD1}|$	V_o	V_o
$|V_{OD2}|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$|V_{OD3}|$		V_t (test termination measurement 2)
$\Delta|V_{OD}|$	$|~|V_t| - |\overline{V}_t|~|$	$|~|V_t - \overline{V}_t|~|$
V_{OC}	$|V_{os}|$	$|V_{os}|$
$\Delta|V_{OC}|$	$|V_{os} - \overline{V}_{os}|$	$|V_{os} - \overline{V}_{os}|$
I_{OS}	$|I_{sal}|$, $|I_{sb}|$	
I_O	$|I_{xa}|$, $|I_{xb}|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = –400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V, See Note 7	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 7: This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

PARAMETER MEASUREMENT INFORMATION
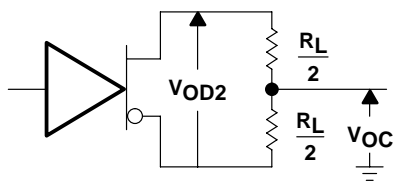
Figure 1. Driver V_{OD} and V_{OC}
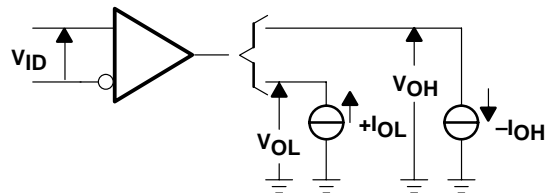
Figure 2. Receiver V_{OH} and V_{OL}
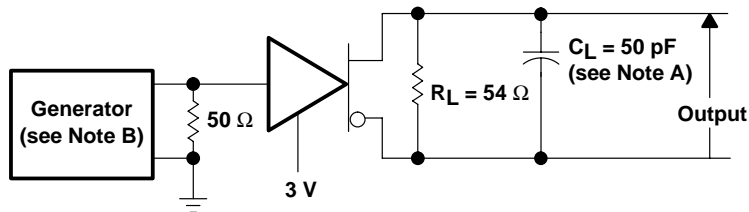
TEST CIRCUIT
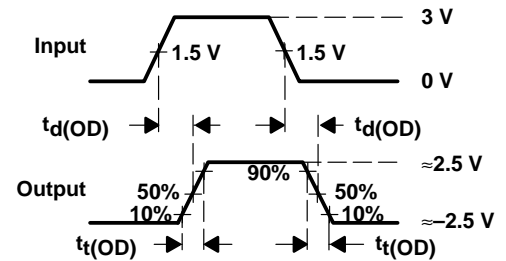
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
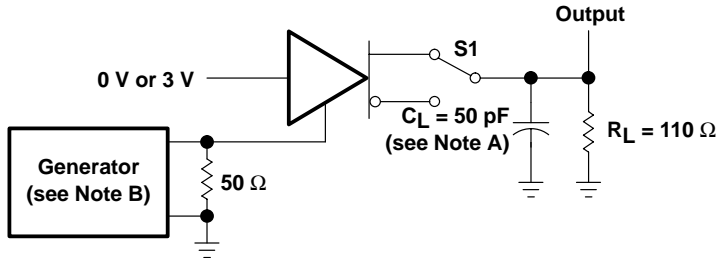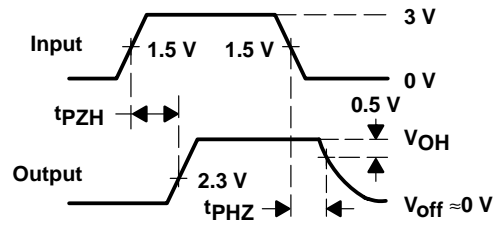
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms
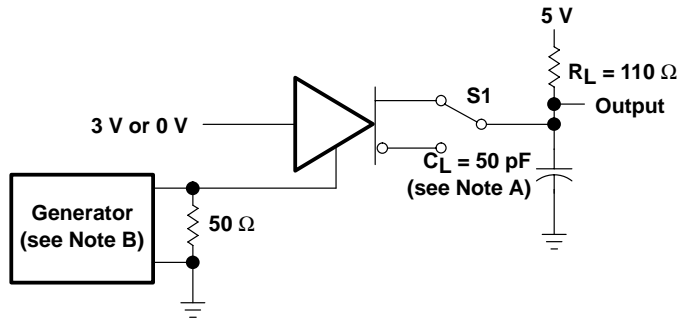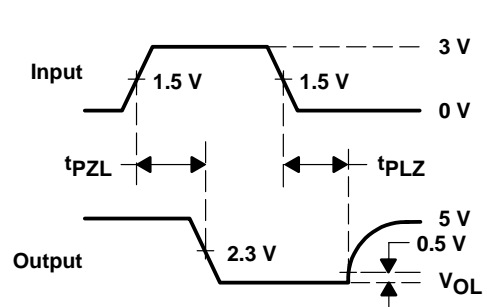
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 5. Driver Test Circuit and Voltage Waveforms
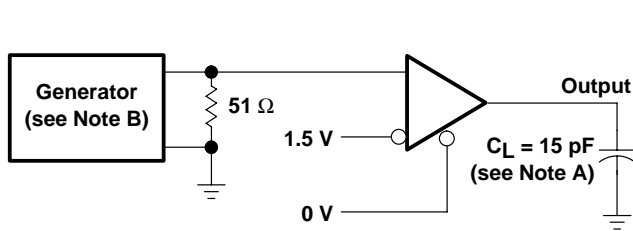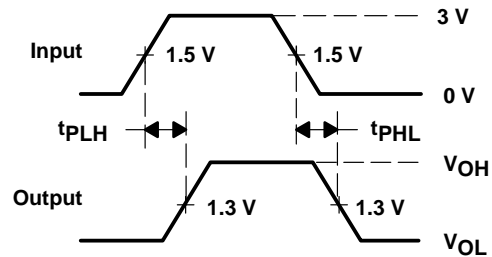
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C
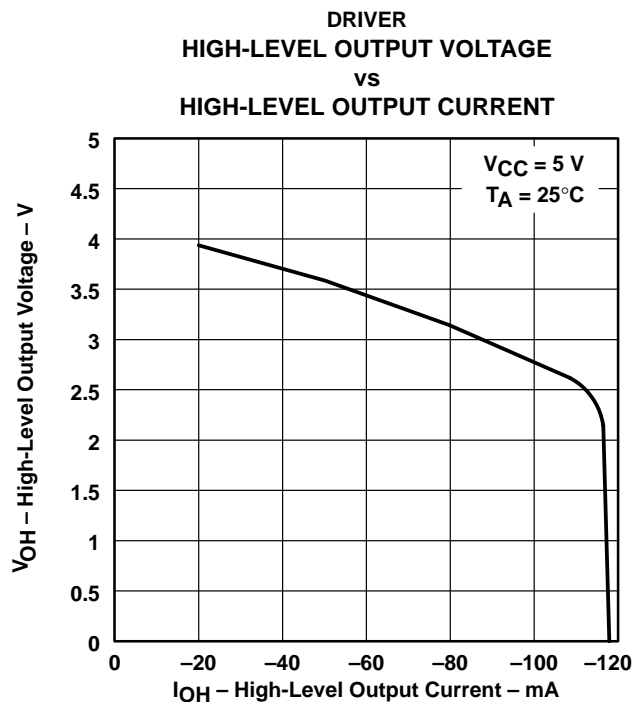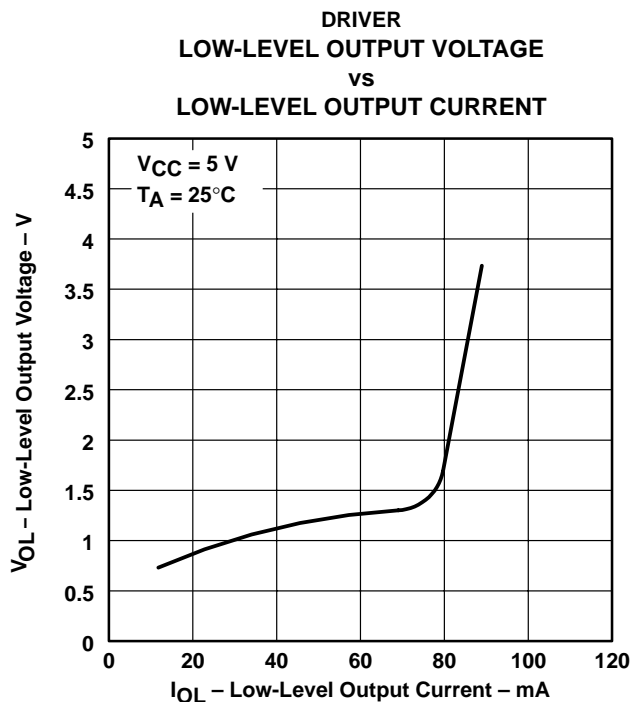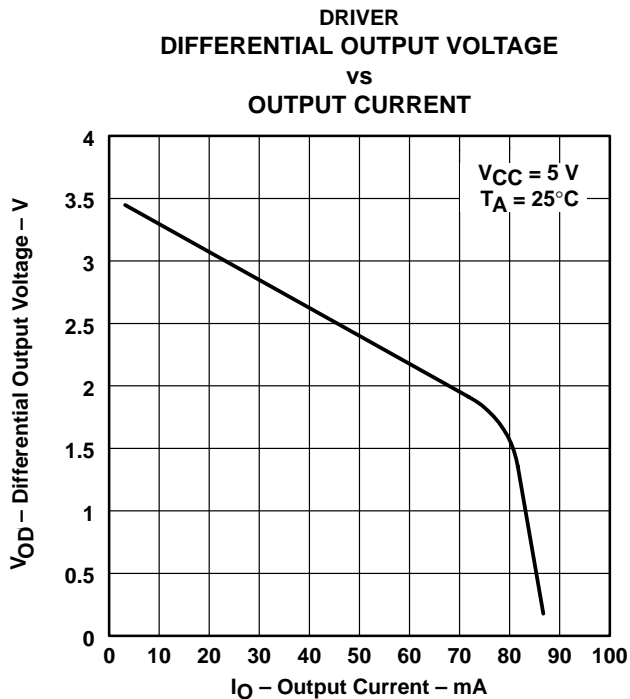
Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†
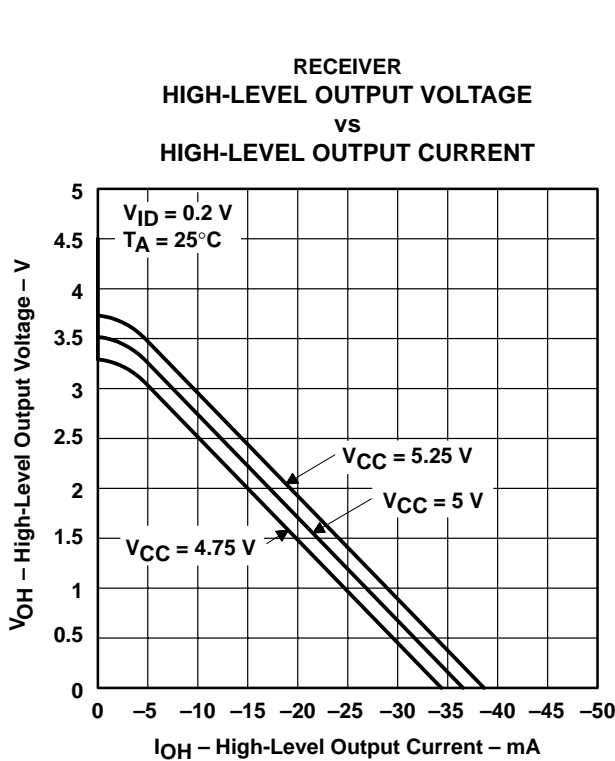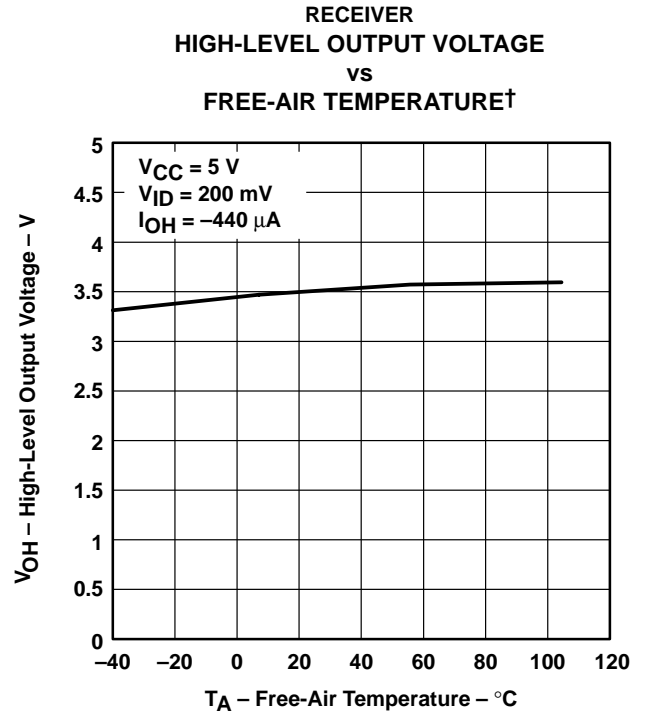
† Only the 0°C to 70°C portion of the curve applies to the SN75176B.

Figure 12
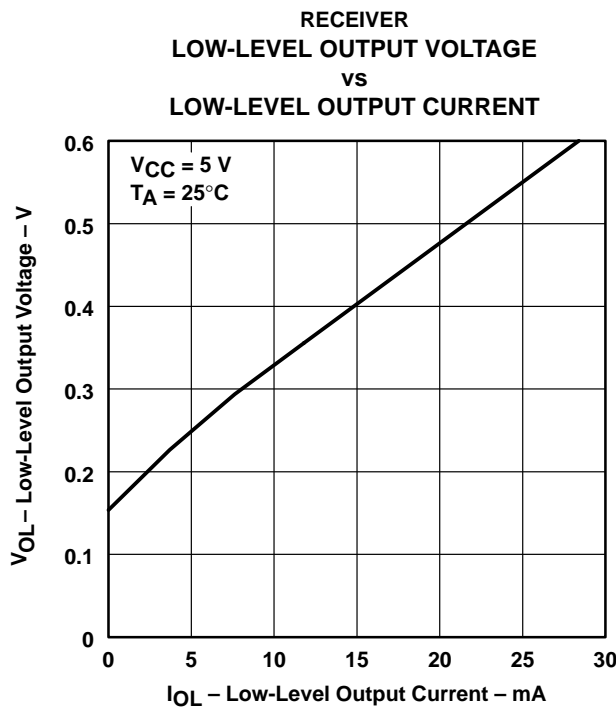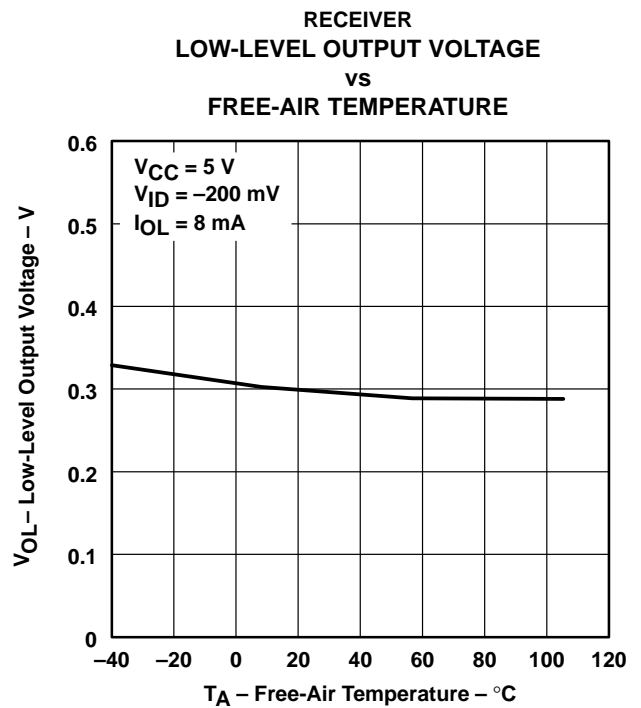
RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 14

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TYPICAL CHARACTERISTICS

**RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE**

V_{ID} = 0.2 V
Load = 8 kΩ to GND
T_A = 25°C

V_{CC} = 5.25 V
V_{CC} = 5 V
V_{CC} = 4.75 V

V_O – Output Voltage – V

V_I – Enable Voltage – V

Figure 15

**RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE**

V_{CC} = 5.25 V
V_{ID} = −0.2 V
Load = 1 kΩ to V_{CC}
T_A = 25°C

V_{CC} = 4.75 V
V_{CC} = 5 V

V_O – Output Voltage – V

V_I – Enable Voltage – V
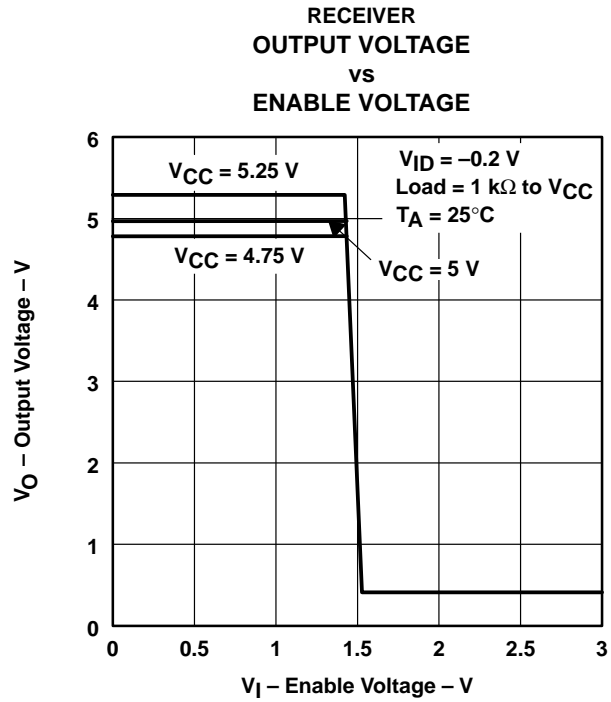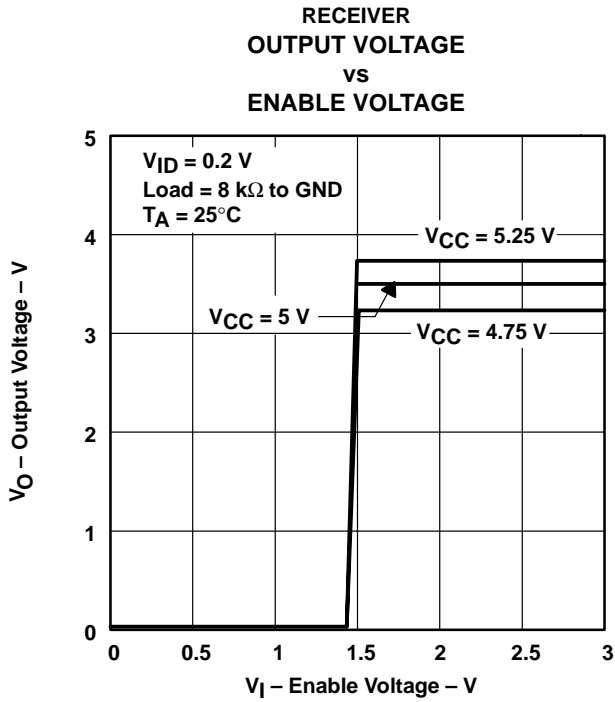
Figure 16

APPLICATION INFORMATION

SN65176B
SN75176B

R_T

R_T

SN65176B
SN75176B

Up to 32
Transceivers
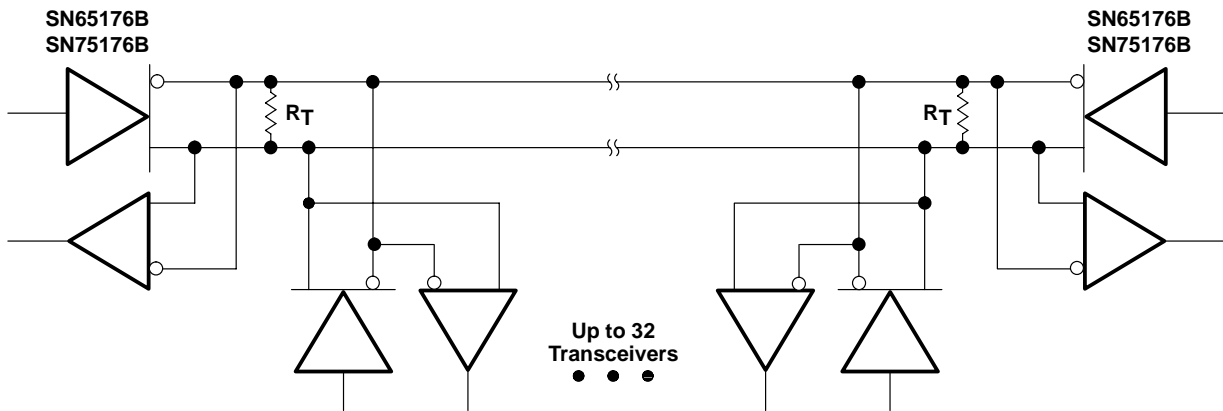
NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65176BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65176BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65176BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75176BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75176BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75176BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
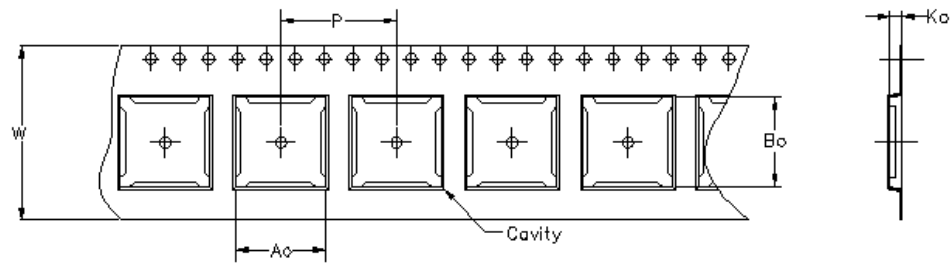
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.

Sprocket Holes

Q1 Q2
Q3 Q4

Q1 Q2
Q3 Q4

Pocket Quadrants
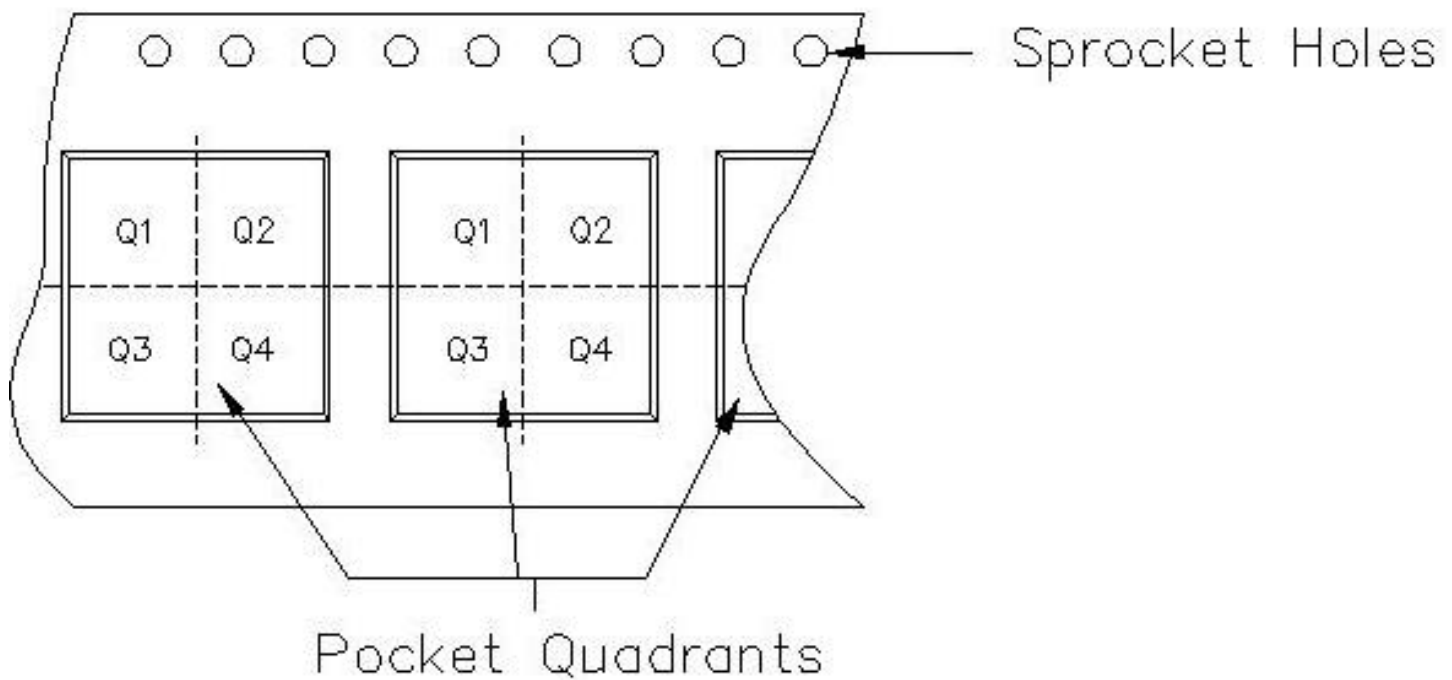
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65176BDR	D	8	FMX	330	12	6.4	5.2	2.1	8	12	Q1
SN75176BDR	D	8	FMX	330	12	6.4	5.2	2.1	8	12	Q1
SN75176BPSR	PS	8	MLA	330	16	8.2	6.6	2.5	12	16	Q1
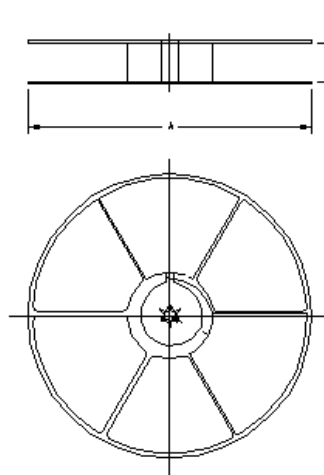
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65176BDR	D	8	FMX	338.1	340.5	20.64
SN75176BDR	D	8	FMX	338.1	340.5	20.64
SN75176BPSR	PS	8	MLA	342.9	336.6	28.58
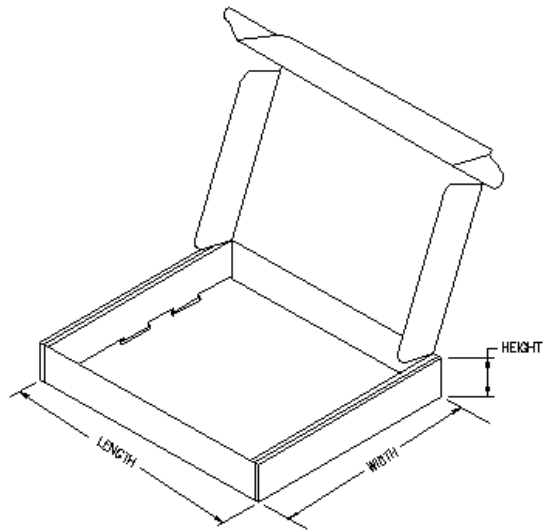
P (R-PDIP-T8)   **PLASTIC DUAL-IN-LINE**

0.400 (10,60)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78) MAX

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gage Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92)
MAX

0.021 (0,53)
0.015 (0,38)   ⊕ | 0.010 (0,25) | Ⓜ

4040082/D 05/98

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE
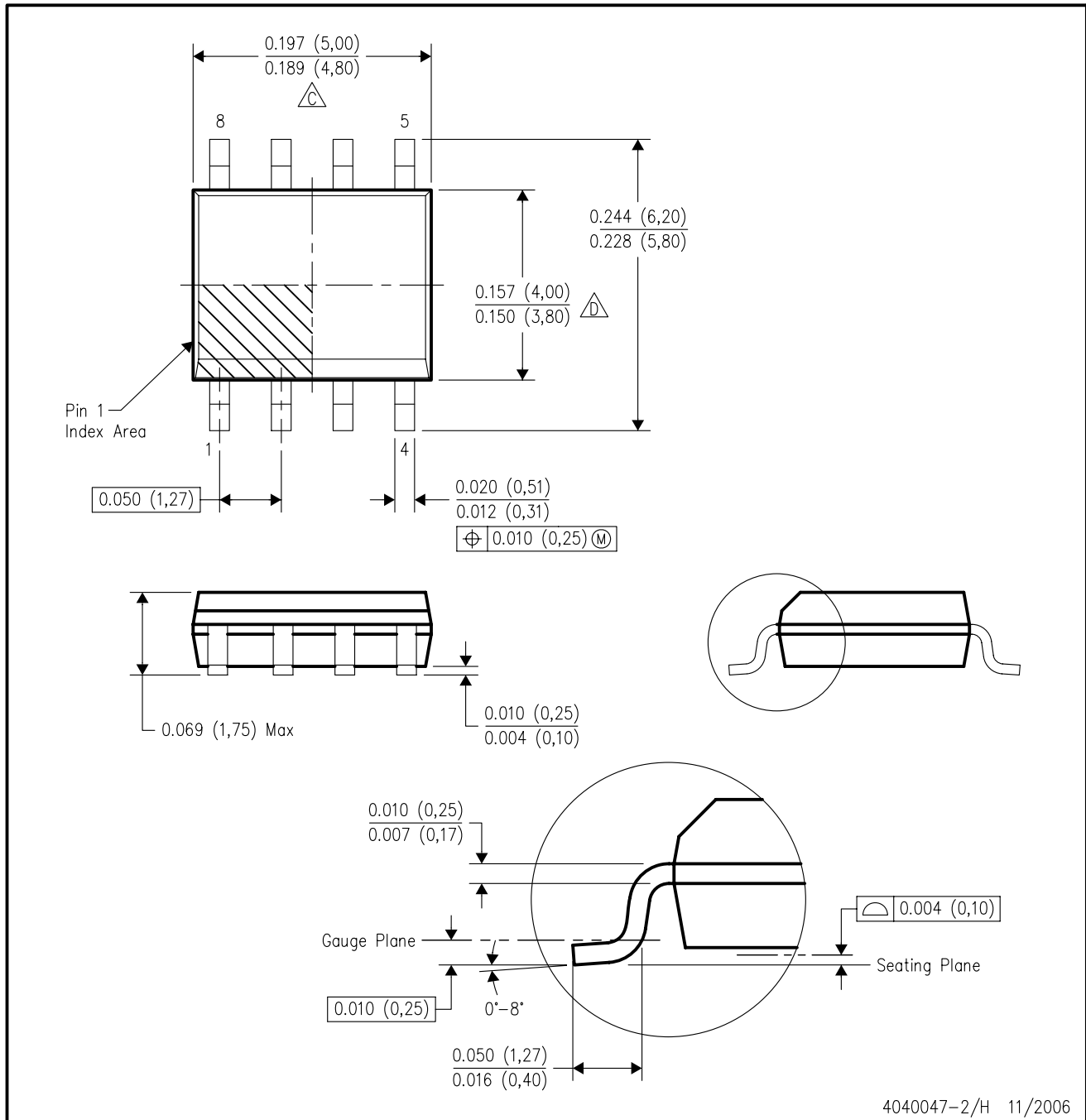
0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Ⓐ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−2/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS−012 variation AA.

MECHANICAL DATA

4040063/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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