SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

# SG1823/SG2823/SG3823

*FUTURE PRODUCT RELEASE*

# HIGH-SPEED CURRENT-MODE PWM

## DESCRIPTION

The SG1823 is a high-performance pulse width modulator optimized for high frequency current-mode power supplies. Included in the controller are a precision voltage reference, micropower start-up circuitry, soft-start, high-frequency oscillator, wideband error amplifier, fast current-limit comparator, full double-pulse suppression logic, and a single totem-pole output driver. Innovative circuit design and an advanced linear Schottky process result in very short propagation delays through the current limit comparator, logic, and the output driver. This device can be used to implement either current-mode or voltage-mode switching power supplies. This device is an ideal choice for applications such as single ended boost converters. The SG1823 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2823 is characterized for the industrial range of -25°C to 85°C, and the SG3823 is selected for the commercial range of 0°C to 70°C.

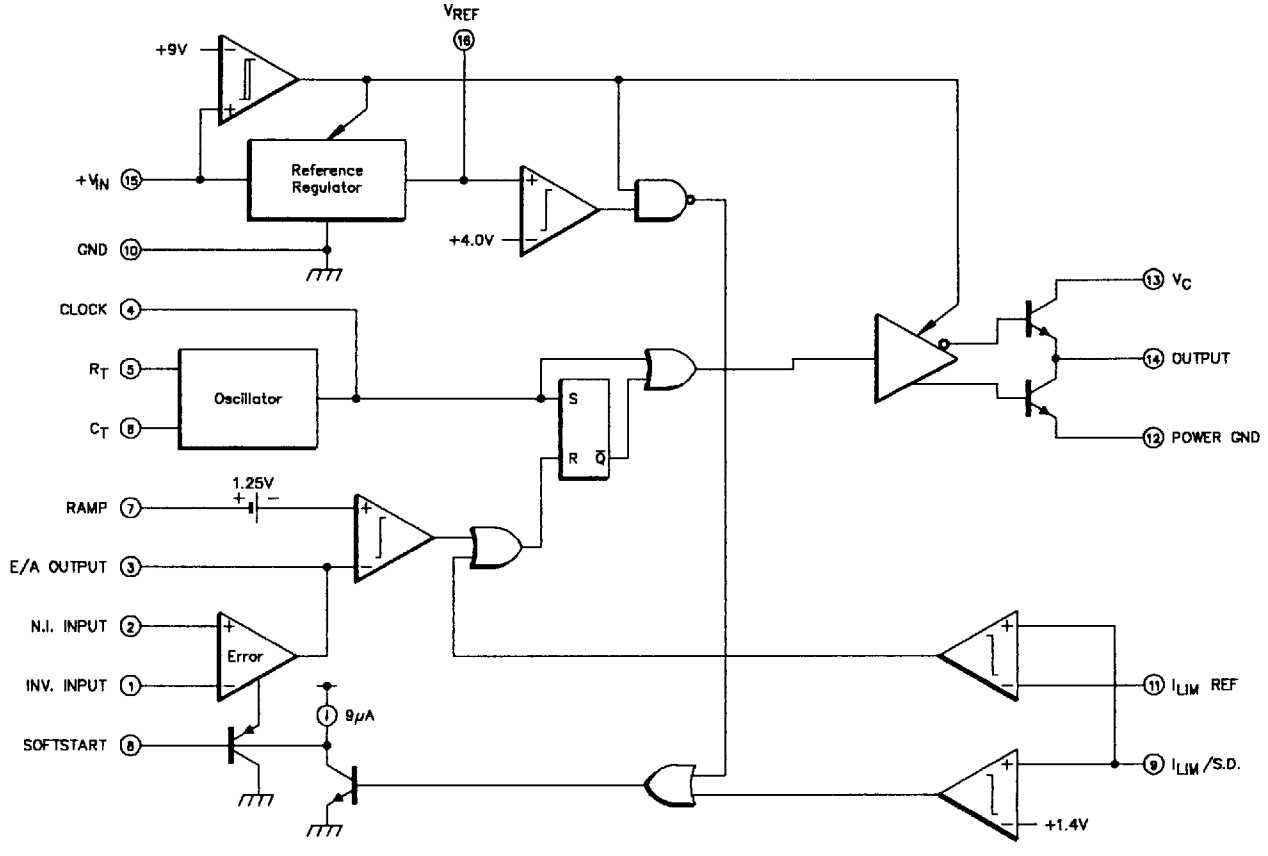
## FEATURES

- **10 to 30 volt operation**
- **5.1V reference trimmed to ±1%**
- **2MHz oscillator capability**
- **80ns prop delay to outputs**
- **1.5A peak totem-pole driver**
- **2mA max start-up current**
- **U.V. lockout with hysteresis**
- **No output driver "float"**
- **Programmable soft start**
- **Double-pulse suppression logic**
- **Wideband low-impedance error amp**
- **Current-mode or voltage-mode control**
- **Wide choice of high frequency packages**

### HIGH RELIABILITY FEATURES - SG1823

- **Available to MIL-STD-883B**
- **SG level "S" processing available**

## BLOCK DIAGRAM



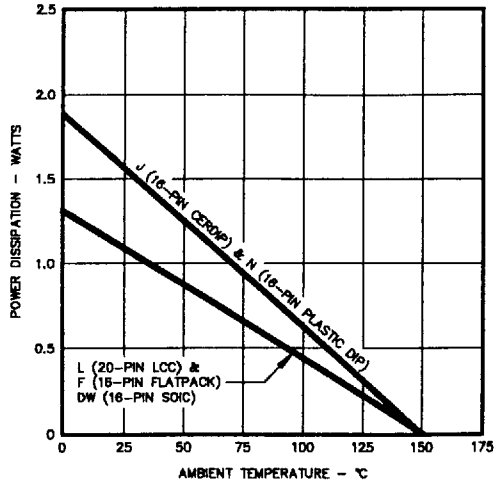

September 1992

## ABSOLUTE MAXIMUM RATINGS (Note 1)

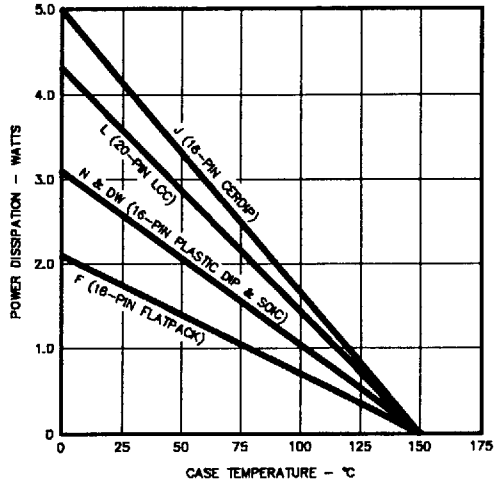
Input Voltage ($V_{IN}$ and $V_C$) ..... 30V
Analog Inputs:
  Error Amplifier and Ramp ..... -0.3V to 7.0V
  Soft Start and $I_{LIM}$/S.D. ..... -0.3V to 6.0V
Digital Input (Clock) ..... 1.5V to 6.0V
Driver Outputs ..... -0.3V to $V_C$+1.5V
Source / Sink Output Current (each output):
  Continuous ..... 0.5A
  Pulse, 500ns ..... 2.0A
Soft Start Sink Current ..... 20mA
Clock Output Current ..... 5mA
Error Amplifier Output Current ..... 5mA
Oscillator Charging Current ..... 5mA
Operating Junction Temperature:
  Hermetic (F, J, L Packages) ..... 150°C
  Plastic (DW, N Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES




MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE




MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

## RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range ..... 10V to 30V
Voltage Amp Common Mode Range ..... 1.5V to 5.5V
Ramp Input Voltage Range ..... 0V to 5.0V
Current Limit / Shutdown Voltage Range ..... 0V to 4.0V
Source / Sink Output Current
  Continuous ..... 200mA
  Pulse, 500ns ..... 1.0A
Voltage Reference Output Current ..... 1 mA to 10mA
Oscillator Frequency Range ..... 4KHz to 1.5MHz
Oscillator Charging Current ..... 30µA to 3mA
Oscillator Timing Resistor ($R_T$) ..... 1KΩ to 100KΩ
Oscillator Timing Capacitor ($C_T$) ..... 470pF to .01µF
Operating Ambient Temperature Range:
  SG1823 ..... -55°C to 125°C
  SG2823 ..... -25°C to 85°C
  SG3823 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

## ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1823 with -55°C ≤ $T_A$ ≤ 125°C, SG2823 with -25°C ≤ $T_A$ ≤ 85°C, SG3823 with 0°C ≤ $T_A$ ≤ 70°C, and $V_{IN}$ = $V_C$ = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

| Parameter | Test Conditions | SG1823/2823 | | | SG3823 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| **Reference Section** | | | | | | | | |
| Output Voltage | $T_J$ = 25°C, $I_L$ = 1mA | 5.05 | 5.10 | 5.15 | 5.00 | 5.10 | 5.20 | V |
| Line Regulation | $V_{IN}$ = 10 to 30V | | 2 | 20 | | 2 | 20 | mV |
| Load Regulation | $I_L$ = 1 to 10mA | | 5 | 20 | | 5 | 20 | mV |
| Temperature Stability (Note 3) | Over Operating Temperature | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/°C |
| Total Output Range (Note 3) | Over Line, Load, and Temperature | 5.00 | | 5.20 | 4.95 | | 5.25 | V |
| Output Noise Voltage (Note 3) | f = 10Hz to 10KHz, $I_L$ = 0mA | | 50 | 200 | | 50 | | $\mu V_{RMS}$ |
| Long Term Stability (Notes 3 & 4) | $T_J$ = 125°C, t = 1000hrs | | 5 | 25 | | 5 | 25 | mV |
| Short Circuit Current | $V_{REF}$ = 0V | -15 | -50 | -100 | -15 | -50 | -100 | mA |

## ELECTRICAL SPECIFICATIONS (continued)

| Parameter | Test Conditions | SG1823/2823 | | | SG3823 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| **Oscillator Section** (Note 5) | | | | | | | | |
| Initial Accuracy | $T_J$ = 25°C, $C_{CLK} \leq$ 10pF | 360 | 400 | 440 | 360 | 400 | 440 | KHz |
| Voltage Stability | $V_{IN}$ = 10 to 30V | | 0.2 | 2 | | 0.2 | 2 | % |
| Temperature Stability (Note 3) | Over Rated Operating Temperature | | 5 | 8 | | 5 | 8 | % |
| Total Frequency Limits (Note 3) | Over Line and Temperature | 340 | | 460 | 340 | | 460 | KHz |
| Minimum Frequency | $R_T$ = 100KΩ, $C_T$ = .01µF | | | 4 | | | 4 | KHz |
| Maximum Frequency | $R_T$ = 1KΩ, $C_T$ = 470pF | 1.5 | | | 1.5 | | | MHz |
| Clock High Level | $I_{CLK}$ = -1mA | 3.9 | 4.5 | | 3.9 | 4.5 | | V |
| Clock Low Level | $I_{CLK}$ = -1mA | | 2.3 | 2.9 | | 2.3 | 2.9 | V |
| Ramp Peak Voltage | | 2.6 | 2.8 | 3.0 | 2.6 | 2.8 | 3.0 | V |
| Ramp Valley Voltage | | 0.7 | 1.0 | 1.25 | 0.7 | 1.0 | 1.25 | V |
| Valley-to-Peak Amplitude | | 1.6 | 1.8 | 2.0 | 1.6 | 1.8 | 2.0 | V |
| **Error Amplifier Section** (Note 6) | | | | | | | | |
| Input Offset Voltage | $R_S \leq$ 2KΩ, $V_{ERROR}$ = 2.5V | | | 10 | | | 15 | mV |
| Input Bias Current | $V_{ERROR}$ = 2.5V | | 0.6 | 3 | | 0.6 | 3 | µA |
| Input Offset Current | $V_{ERROR}$ = 2.5V | | 0.1 | 1 | | 0.1 | 1 | µA |
| DC Open Loop Gain | $V_{ERROR}$ = 1 to 4V | 60 | 95 | | 60 | 95 | | dB |
| Common Mode Rejection | Over Rated Voltage Range, $V_{ERROR}$ = 2.5V | 75 | 95 | | 75 | 95 | | dB |
| Power Supply Rejection | $V_{IN}$ = 10V to 30V, $V_{ERROR}$ = 2.5V | 85 | 110 | | 85 | 110 | | dB |
| Output Sink Current | $V_{ERROR}$ = 1V | 1 | 2.5 | | 1 | 2.5 | | mA |
| Output Source Current | $V_{ERROR}$ = 4V | -0.5 | -1.3 | | -0.5 | -1.3 | | mA |
| Output High Voltage | $I_{ERROR}$ = -0.5mA | 4.0 | 4.7 | 5.0 | 4.0 | 4.7 | 5.0 | V |
| Output Low Voltage | $I_{ERROR}$ = 1mA | 0 | 0.5 | 1.0 | 0 | 0.5 | 1.0 | V |
| Unity Gain Bandwidth (Note 3) | $A_{VOL}$ = 0dB | 3 | 5.5 | | 3 | 5.5 | | MHz |
| Slew Rate (Note 3) | | 6 | 12 | | 6 | 12 | | V/µsec |
| **PWM Comparator Section** (Note 5 & 7) | | | | | | | | |
| Ramp Input Bias Current | | | -1 | -5 | | -1 | -5 | µA |
| Minimum Duty Cycle | $V_{ERROR}$ = 1V | | | 0 | | | 0 | % |
| Maximum Duty Cycle (Note 8) | $V_{ERROR}$ = 4V | 85 | | | 85 | | | % |
| Zero Duty Cycle Threshold | | 1.1 | 1.25 | | 1.1 | 1.25 | | V |
| Delay to Driver Output (Note 3) | $V_{RAMP}$ = 0 to 2V, $V_{ERROR}$ = 2V | | 50 | 80 | | 50 | 80 | ns |
| **SoftStart Section** | | | | | | | | |
| $C_{SS}$ Charge Current | $V_{SOFTSTART}$ = 0.5V | 3 | 9 | 20 | 3 | 9 | 20 | µA |
| $C_{SS}$ Discharge Current | $V_{SOFTSTART}$ = 1.0V | 1 | | | 1 | | | mA |
| **Current Limit / Shutdown Section** (Note 9) | | | | | | | | |
| $I_{LIM}$/S.D. Input Bias Current | | | | ±10 | | | ±10 | µA |
| $I_{LIM}$ REF Offset | $V_{ILIM}$ = 1.1V | | | 15 | | | 15 | mV |
| $I_{LIM}$ REF Common Mode Range | | 1.0 | | 1.25 | 1.0 | | 1.25 | V |
| Shutdown Threshold | $V_{SHUTDOWN}$ = 0V to 1.2V | 1.25 | 1.40 | 1.55 | 1.25 | 1.40 | 1.55 | V |
| Delay to Driver Output (Note 3) | | | 50 | 80 | | 50 | 80 | ns |
| **Output Drivers (each output)** | | | | | | | | |
| Output Low Level | $I_{SINK}$ = 20mA | | 0.25 | 0.40 | | 0.25 | 0.40 | V |
| | $I_{SINK}$ = 200mA | | 1.2 | 2.2 | | 1.2 | 2.2 | V |
| Output High Level | $I_{SOURCE}$ = 20mA | 13.0 | 13.5 | | 13.0 | 13.5 | | V |
| | $I_{SOURCE}$ = 200mA | 12.0 | 13.0 | | 12.0 | 13.0 | | V |
| $V_C$ Standby Current | $V_C$ = 30V | | 150 | 500 | | 150 | 500 | µA |
| Output Rise / Fall Time (Note 3) | $C_L$ = 1000pF | | 30 | 60 | | 30 | 60 | ns |
| **Undervoltage Lockout Section** | | | | | | | | |
| Start Threshold Voltage | | 8.8 | 9.2 | 9.6 | 8.8 | 9.2 | 9.6 | V |
| UV Lockout Hysteresis | | 0.4 | 0.8 | 1.2 | 0.4 | 0.8 | 1.2 | V |
| **Supply Current Section** (Note 5) | | | | | | | | |
| Start Up Current | $V_{IN}$ = 8V | | 1.1 | 2.5 | | 1.1 | 2.5 | mA |
| Operating Current | $V_{INV}$, $V_{RAMP}$, $V(I_{LIM}/S.D.)$ = 0V, $V_{N.I.}$ = 1V | | 22 | 33 | | 22 | 33 | mA |

Note 3. This parameter is guaranteed by design and process control, but is not 100% tested in production.
Note 4. This parameter is non-accum., and represents the random fluctuation of the ref. voltage within some error band when observed over any 1000 hr. period of time.

Note 5. $F_{OSC}$ = 400KHz ($R_T$ = 3.65KΩ, $C_T$ = 1.0nF)
Note 6. $V_{CM}$ = 1.5V to 5.5V.
Note 7. $V_{RAMP}$ = 0V, unless otherwise specified.
Note 8. 100% duty cycle is defined as a pulsewidth equal to one oscillator period.
Note 9. $V(I_{LIM}/SHUTDOWN)$ = 0V to 4.0V, unless otherwise specified.

## APPLICATION INFORMATION

### HIGH-SPEED LAYOUT AND BYPASSING

The SG1823, like all high-speed circuits, requires extra attention to external conductor and component layout to minimize undesired inductive and capacitive effects. All lead lengths must be as short as possible. The best printed circuit board choice would be a four-layer design, with the two internal planes supplying power and ground. Signal interconnects should be placed on the outside, giving a conductor-over-ground-plane (microstrip) configuration. A two-sided pc board with one side dedicated as a ground plane is next best, and requires careful component placement by a skilled pc designer.

Two supply bypass capacitors should be employed: a low-inductance 0.1 µF ceramic within 0.25 inches of the $+V_{IN}$ pin for high frequencies, and a 1 to 5 µF solid tantalum within 0.5 inches of the $V_C$ pin to provide an energy reservoir for the high peak output currents. A low-inductance .01 µF bypass for the reference output is also recommended.

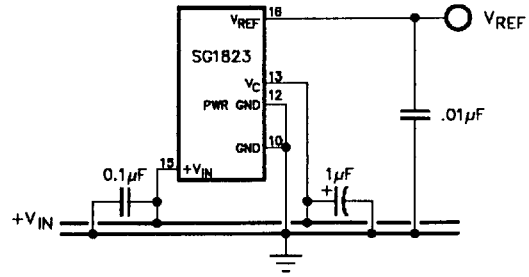



FIGURE 1
HIGH SPEED LAYOUT AND BYPASSING

### MICROPOWER STARTUP

Since the SG1823 draws less than 2.5 mA of supply current before turning on, a low power bleeder resistor from the rectified AC line supply is all that is required for startup. A start capacitor, $C_S$, is charged with the excess current from the bleeder resistor. When the turn-on threshold voltage is reached, the PWM circuit becomes active, energizing the power transistors. The additional operating current required by the PWM is then provided by a bootstrap winding on the main high-frequency power transformer.

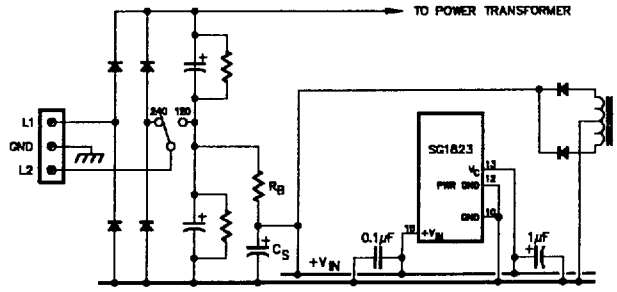



FIGURE 2
MICROPOWER STARTUP

### SOFTSTART CIRCUIT / OUTPUT DUTY CYCLE LIMIT

The Softstart pin of the SG1823 is held low when either the chip is in the micropower mode, or when a voltage greater than +1.4 volts is present at the $I_{LIM/S\,D}$ pin. The maximum positive swing of the voltage error amplifier is clamped to the Softstart pin voltage, providing a ramp-up of peak charging currents in the power semiconductors at turn-on.

In some cases, the duration of the Shutdown signal can be too short to fully discharge the softstart capacitor. The illustrated resistor/discrete PNP transistor configuration can be used to shorten the discharge time by a factor of 50 or more. When the internal discharge transistor in the SG1825 turns on, current will flow through surge limit resistor R1. As the resistor drop approaches 0.6 volts, the external PNP turns on, providing a low resistance discharge path for the energy in the softstart capacitor. The capacitor will be rapidly discharged to +0.7 volts, which corresponds to zero duty cycle in the pulse width modulator.

To program the maximum output duty cycle, a resistor divider shold be connected from the $V_{REF}$ pin to the Soft Start pin. A resistor divider combination ($R_2 + R_3$) of less than 5KΩ achieves better than 2% voltage tolerance at the Soft Start pin.

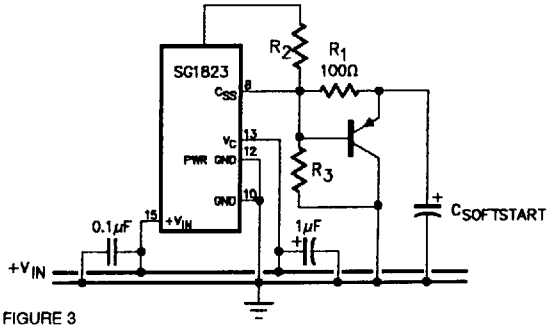



FIGURE 3
SOFTSTART FAST RESET

### FREQUENCY SYNCHRONIZATION

Two or three SG1823 oscillators may be locked together with the interconnection scheme shown, if the devices are within an inch or so of each other. A master unit is programmed for desired frequency with $R_T$ and $C_T$ as usual. The oscillators in the slave units are disabled by grounding $C_T$ and by connecting $R_T$ to $V_{REF}$. The logic in the slave units is locked to the clock of the master with the wire-OR connection shown.

Many SG1825s can be locked to a master system clock by wiring the oscillators as slave units, and distributing the master clock to each using a tree-fanout geometry.

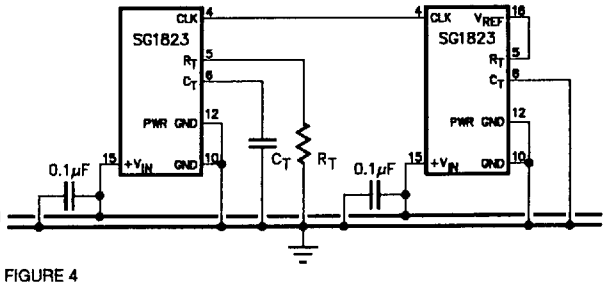



FIGURE 4
OSCILLATOR SYNCHRONIZATION

## APPLICATION INFORMATION

### OSCILLATOR

The oscillator frequency is programmed by external timing components $R_T$ and $C_T$. A nominal +3.0 volts appears at the $R_T$ pin. The current flowing through $R_T$ is mirrored internally with a 1:1 ratio. This causes an identical current to flow out the $C_T$ pin, charging the timing capacitor and generating a linear ramp. When the upper threshold of +2.8 volts is reached, a discharge network reduces the ramp voltage to +1.0, where a new charge cycle begins.

The Clock output pin is LOW (+2.3 volts) during the charge cycle, and HIGH (+4.5 volts) during the discharge cycle. The Clock pin is driven by an NPN emitter follower, and so can be wire-ORed. Each Clock pin can drive a 1 mA load. Since the internal current-source pulldown is approximately 400 µA, the DC fan-out to other SG1825 Clock pins is at least two.

The type of capacitor selected for $C_T$ is very important. At high frequencies, non-ideal characteristics such as effective series resistance (ESR), effective series inductance (ESL), dielectric loss and dielectric absorption all affect frequency accuracy and stability. RF capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. Avoid high-K ceramics, which work best in DC bypass applications.

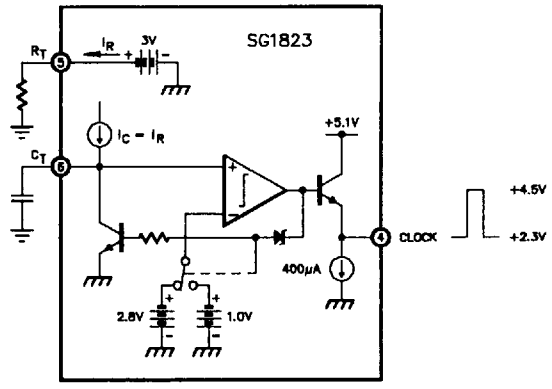



FIGURE 5
OSCILLATOR FUNCTIONAL DIAGRAM

### ERROR AMPLIFIER

The voltage error amplifier is a true operational amplifier with low-impedance output, and can be gain-stabilized using conventional feedback techniques. The typical DC open-loop gain is 95 dB, with a single low-frequency pole at 100 Hz.

The input connections to the error amplifier are determined by the polarity of the power supply output voltage. For positive supplies, the common-mode voltage is +5.1 volts and the feedback connections in Figure A are used. With negative outputs, the common-mode voltage is half the reference, and the feedback divider is connected between the negative output and the +5.1 volt reference as shown in Figure B.

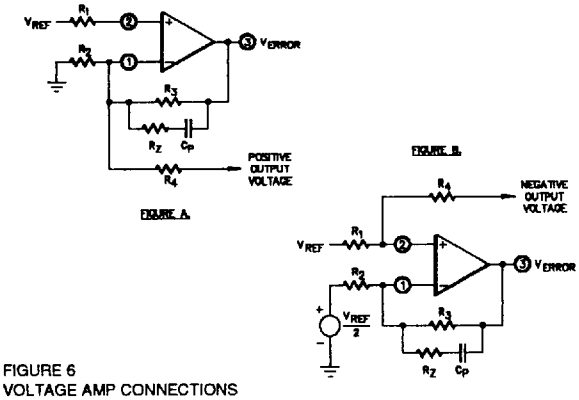



FIGURE 6
VOLTAGE AMP CONNECTIONS

### OUTPUT DRIVER

The output driver is designed to provide up to 1.5 Amps peak output current. To minimize ringing on the output waveform, which can be destructive to both the power MOSFET and the PWM chip, the series inductance seen by the drivers should be as low as possible.

One solution is to keep the distance between the PWM and MOSFET gate as short as possible, and to use carbon composition series damping resistors. A Faraday shield to intercept radiated EMI from the power transistors is usually required with this choice.

A second approach is to place the MOSFETs some distance from the PWM chip, and use a series-terminated transmission line to preserve drive pulse fidelity. This will minimize noise radiated back to the sensitive analog circuitry of the SG1823. A Faraday shield may also be required.

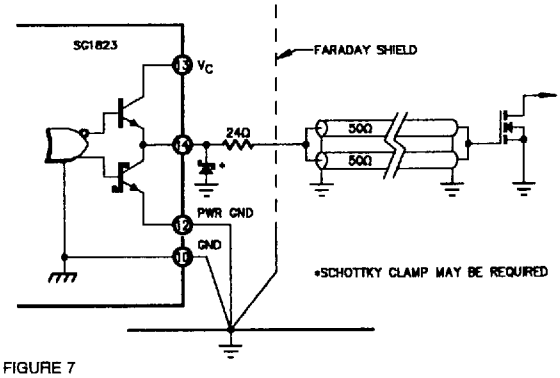
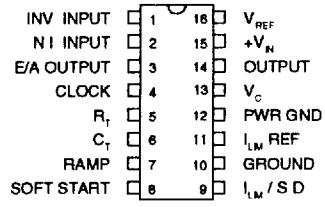
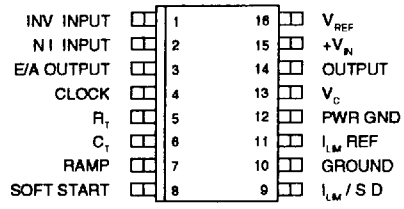
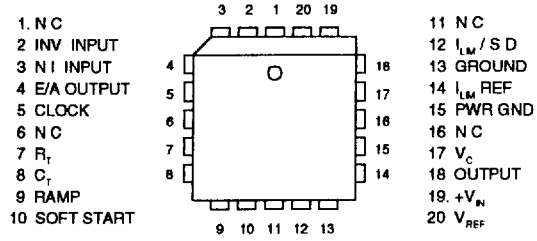



FIGURE 7
DRIVING SHIELDED CABLE

If the driver is connected to an isolation transformer, or if kickback through $C_{GD}$ of the MOSFET is severe, clamp diodes may be required. 1 Amp peak Schottky diodes will limit undershoot to less than -0.3 volts.

## CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

| Package | Part No. | Ambient Temperature Range | Connection Diagram |
|---|---|---|---|
| 16-PIN CERAMIC DIP<br>J - PACKAGE | SG1823J/883B<br>SG1823J<br>SG2823J<br>SG3823J | -55°C to 125°C<br>-55°C to 125°C<br>-25°C to 85°C<br>0°C to 70°C |  |
| 16-PIN PLASTIC DIP<br>N - PACKAGE | SG2823N<br>SG3823N | -25°C to 85°C<br>0°C to 70°C | |
| 16-PIN WIDE BODY<br>PLASTIC S.O.I.C.<br>DW - PACKAGE | SG2823DW<br>SG3823DW | -25°C to 85°C<br>0°C to 70°C |  |
| 20-PIN PLASTIC<br>LEADED CHIP CARRIER<br>Q- PACKAGE<br>(Note 3) | SG2823Q<br>SG3823Q | -25°C to 85°C<br>0°C to 70°C |  |





Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Contact factory for package availabiility