SIEMENS

SFH6138
SFH6139

LOW INPUT CURRENT, HIGH GAIN TRIOS®* OPTOCOUPLER

FEATURES

- **High Current Transfer Ratio, 800%**
- **Low Input Current Requirement, 0.5mA**
- **High Output Current, 60mA**
- **Withstand Test Voltage, 5300 VDC**
- **TTL Compatible Output, 0.1V V_{OL}**
- **High Common Mode Rejection, 500V/µsec.**
- **DC to 0.1 Megabit/Sec. Operation**
- **Adjustable Bandwidth–Access to Base**
- **Standard Molded Dip Plastic Package**
- **Underwriters Lab File #E52744**
- **Option 1 Available: VDE Approval #0884**

APPLICATIONS

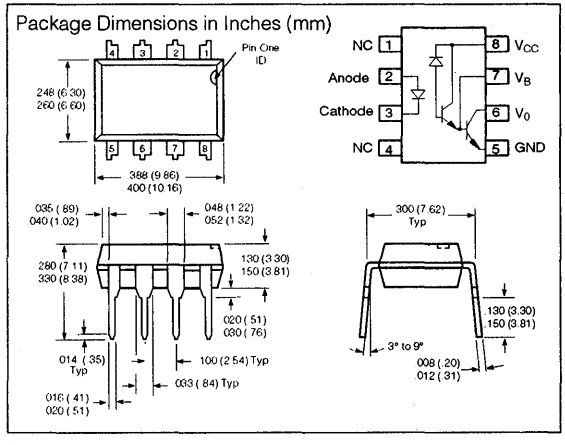
- **Logic Ground Isolation–TTL/TTL, TTL/CMOS, CMOS/CMOS, CMOS/TTL**
- **EIA RS 232C Line Receiver**
- **Low Input Current Line Receiver–Long Lines, Party Lines**
- **Telephone Ring Detector**
- **117 VAC Line Voltage Status Indication–Low Input Power Dissipation**
- **Low Power Systems–Ground Isolation**

DESCRIPTION

High common mode transient immunity and very high current ratio together with 5300 VDC insulation are achieved by coupling an LED with an integrated high gain photon detector in an eight pin dual-in-line package. Separate pins for the photodiode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the V_{CC} and V_O terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

The SFH6138 is ideal for TTL applications since the 300% minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 KΩ pull-up resistor.

The SFH6139 is best suited for low power logic applications involving CMOS and low power TTL. A 400% current transfer ratio with only 0.5 mA of LED current is guaranteed from 0°C to 70°C.



Maximum Ratings

Reverse Input Voltage ..... 5 V
Supply and Output Voltage, V_{CC} (pin 8-5), V_O (pin 6-5)
SFH6138 ..... –0.5 to 7 V
SFH6139 ..... –0.5 to 18 V
Emitter-Base Reverse Voltage (pin 5-7) ..... 0.5 V
Average Input Current ..... 20 mA
Peak Input Current ..... 40 mA
(50% Duty Cycle–1 ms pulse width)
Peak Transient Input Current
(tp≤1 µsec, 300 pps ..... 1.0 A
Output Current I_O (pin 6) ..... 60 mA
Derate linearly above 25°C, free air temperature at 0.7 mA/°C
Input Power Dissipation ..... 35 mW
Derate linearly above 50%, free air temperature at 0.7 mW/°C
Output Power Dissipation ..... 100 mW
Derate linearly above 25°C, free air temperature at 0.2 mA/°C
Storage Temperature ..... –55°C to +125°C
Operating Temperature ..... –55°C to +100°C
Lead Soldering Temperature (t=10 sec.) ..... 260°C

***TRIOS–TR**ansparent **IO**n **S**hield

Electro-Optical Characteristics (T_A=0°C to 70°C, unless otherwise specified)

Parameter	Device	Min	Typ	Max	Units	Test Conditions	Note
Current Transfer Ratio (CTR)	SFH6138	300	1600		%	I_F=1.6 mA, V_O=0.4 V, V_{CC}=4.5 V	5,6
	SFH6139	400 500	1600 2000		%	I_F=0.5 mA, V_O=0.4 V, V_{CC}=4.5 V I_F=1.6 mA, V_O=0.4 V, V_{CC}=4.5 V	5,6
Logic Low Output Voltage (VOL)	SFH6138		0.1	0.4	V	I_F=1.6 mA, I_O=4.8 mA, V_{CC}=4.5 V	6
	SFH6139 SFH6139 SFH6139		0.1 0.15 0.25	0.4 0.4 0.4	V	I_F=1.6 mA, I_O=8 mA, V_{CC}=4.5 V I_F=5 mA, I_O=15 mA, V_{CC}=4.5 V I_F=12 mA, I_O=24 mA, V_{CC}=4.5 V	6
Logic High	SFH6138		0.1	250	µA	I_F=0 mA, V_O=V_{CC}=7 V	6
Output Current (I_{OH})	SFH6139		0.05	100	µA	I_F=0 mA, V_O=V_{CC}=18 V	6
Logic Low Supply Current (I_{CCL})			0.2	1.5	mA	I_F=1.6 mA, V_O=OPEN, V_{CC}=18 V	6
Logic High Supply Current (I_{CCH})			0.001	10	µA	I_F=0 mA, V_O=OPEN, V_{CC}=18 V	6
Input Forward Voltage (VF)			1.4	1.7	V	I_F=1.6 mA, T_A=25°C	
Input Reverse Breakdown Voltage (BV_R)		5			V	I_R=10 µA	
Temperature Coefficient of Forward Voltage			-1.8		mV/°C	I_F=1.6 mA	
Input Capacitance (C_{IN})			25		pF	f=1 MHz, V_F=0	
Input-Output Insulation Leakage Current (I-0)				1.0	µA	45% Relative Humidity, T_A=25°C t=5s, V_{I-O}=5300 VDC	7
Resistance (Input-Output) (R_{I-O})			10^{12}		Ω	V_{IO}=500 VDC	7
Capacitance (Input-Output)			0.6		pF	f=1 MHz	7

Switching Specifications (T_A=25°C)

Parameter	Device	Min.	Typ.	Max.	Units	Test Conditions	Note
Propagation Delay Time	SFH6138		2	10	µs	I_F=1.6 mA, R_L=2.2 KΩ	
	SFH6139		6	25	µs	I_F=0.5 mA, R_L=4.7 KΩ	6,8
To Logic Low at Output tPHL			0.6	1		I_F=12 mA, R_L=270 Ω	
Propagation Delay Time	SFH6138		4	35	µs	I_F=1.6 mA, R_L=2.2 KΩ	
	SFH6139		5	60		I_F=0.5 mA, R_L=4.7 KΩ	
To Logic High at Output tPLH			1	7	µs	I_F=12 mA, R_L=270 mAΩ	6,8
Common Mode Transient Immunity at Logic High Level (CM_H) Output			500		V/µs	I_F=0 mA, R_L=2.2 KΩ R_{CC}=0/V_{CM}=10 V_{p-p}	9,10
Common Mode Transient Immunity at Logic Low Level (CM_L) Ouput			-500		V/µs	I_F=1.6 mA, R_L=2.2 KΩ R_{CC}=0/V_{CM}=10 V_{p-p}	9,10

Notes

1. Derate linearly above 50°C free-air temperature at a rate of 0.4 mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7 mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7 mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0 mW/°C.
5. DC current transfer ratio is defined as the ratio of outpput collector current, I_O, to the forward LED input current, I_F times 100%.
6. Pin 7 open.
7. Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.
8. Using a resistor between pin 5 and 7 will decrease gain and delay time.
9. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a logic high state (i.e. V_O>2.0 V) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode puse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e. V_O<0.8 V).
10. In applications where dv/dt may exceed 50,000 V/µs (such as state discharge) a series resistor, R_{CC} should be included to protect I_C from destructively high surge currents. The recommended value is $R_{CC} \geq \frac{IV}{0.15\ I_F\ (mA)}$ kΩ.