MICROCOMPUTER/MICROPROCESSOR PERIPHERAL IC FOR VIEWDATA (LUCY)

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface. • Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parity).
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters. • Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

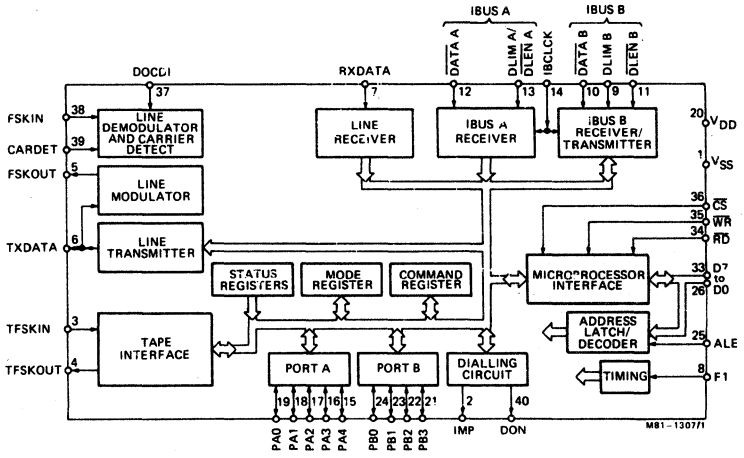
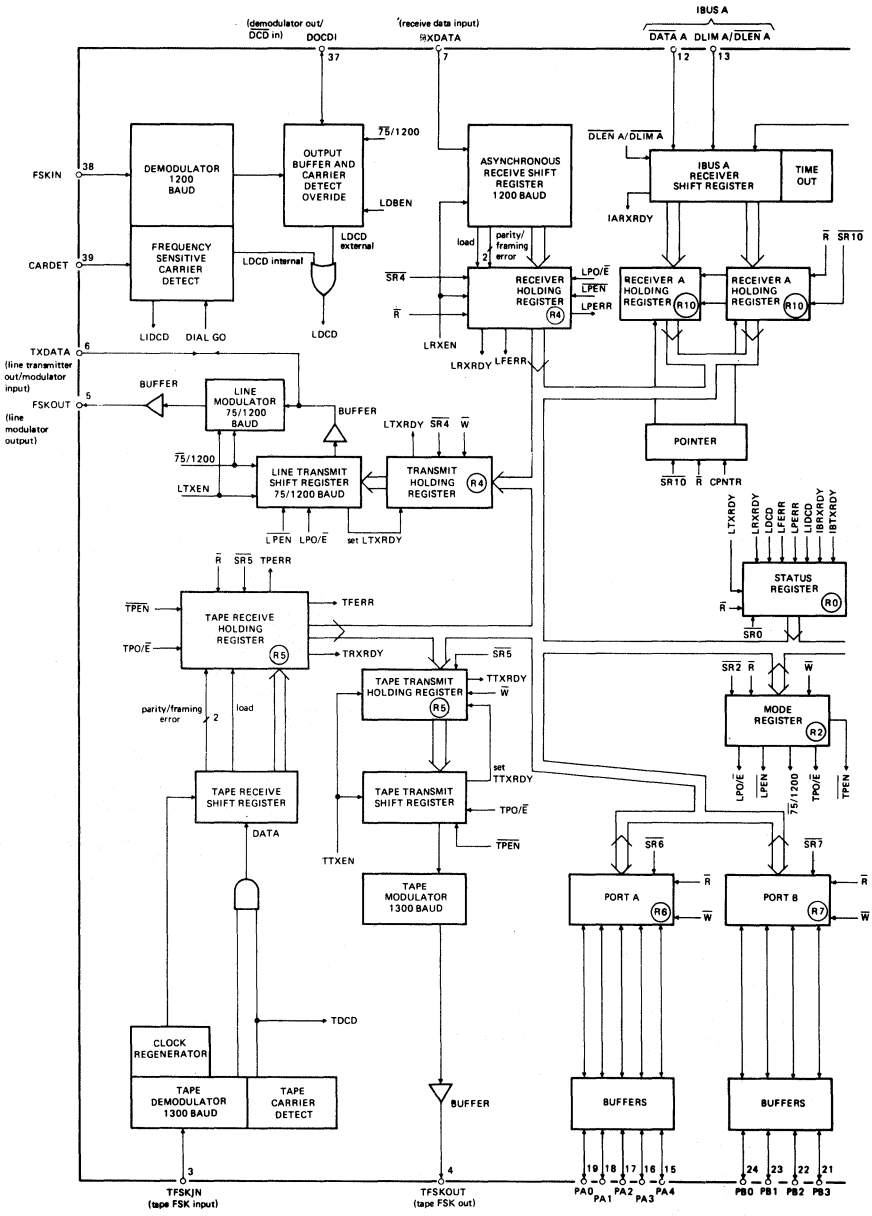


Fig.1a Simplified block diagram

PACKAGE OUTLINE

40-lead DIL; plastic (SOT–129).


(demodulator out/ DCD in)
DOCDI
37
(receive data input)
RXDATA
7
IBUS A
DATA A
DLIM A/DLEN A
12
13
FSKIN
38
DEMODULATOR 1200 BAUD
OUTPUT BUFFER AND CARRIER DETECT OVERIDE
75/1200
LDBEN
ASYNCHRONOUS RECEIVE SHIFT REGISTER 1200 BAUD
DLEN A/DLIM A
IBUS A RECEIVER SHIFT REGISTER
TIME OUT
IARXRDY
CARDET
39
FREQUENCY SENSITIVE CARRIER DETECT
LDCD internal
LDCD external
load
parity/ framing error
2
SR4
RECEIVER HOLDING REGISTER
R4
LPO/E
LPEN
LPERR
RECEIVER A HOLDING REGISTER
R10
R
SR10
LIDCD
DIAL GO
LDCD
LRXEN
LRXRDY
LFERR
TXDATA
6
(line transmitter out/modulator input)
FSKOUT
5
(line modulator output)
BUFFER
LINE MODULATOR 75/1200 BAUD
LTXRDY
SR4
W
POINTER
SR10
R
CPNTR
75/1200
LTXEN
LINE TRANSMIT SHIFT REGISTER 75/1200 BAUD
TRANSMIT HOLDING REGISTER
R4
LPEN
LPO/E
set LTXRDY
LTXRDY
LRXRDY
LDCD
LFERR
LPERR
LIDCD
IBRXRDY
IBTXRDY
STATUS REGISTER
R0
SR0
SR5
TPERR
TPEN
TAPE RECEIVE HOLDING REGISTER
R5
TFERR
TPO/E
TRXRDY
SR5
TAPE TRANSMIT HOLDING REGISTER
R5
TTXRDY
W
SR2
MODE REGISTER
R2
parity/framing error
2
load
set TTXRDY
TAPE RECEIVE SHIFT REGISTER
TAPE TRANSMIT SHIFT REGISTER
TPO/E
TPEN
DATA
TTXEN
SR6
SR7
PORT A
R6
PORT B
R7
TAPE MODULATOR 1300 BAUD
TDCD
CLOCK REGENERATOR
TAPE DEMODULATOR 1300 BAUD
TAPE CARRIER DETECT
BUFFER
BUFFERS
BUFFERS
3
TFSKIN
(tape FSK input)
4
TFSKOUT
(tape FSK out)
19
18
17
16
15
PA0
PA1
PA2
PA3
PA4
24
23
22
21
PB0
PB1
PB2
PB3

DEVELOPMENT DATA

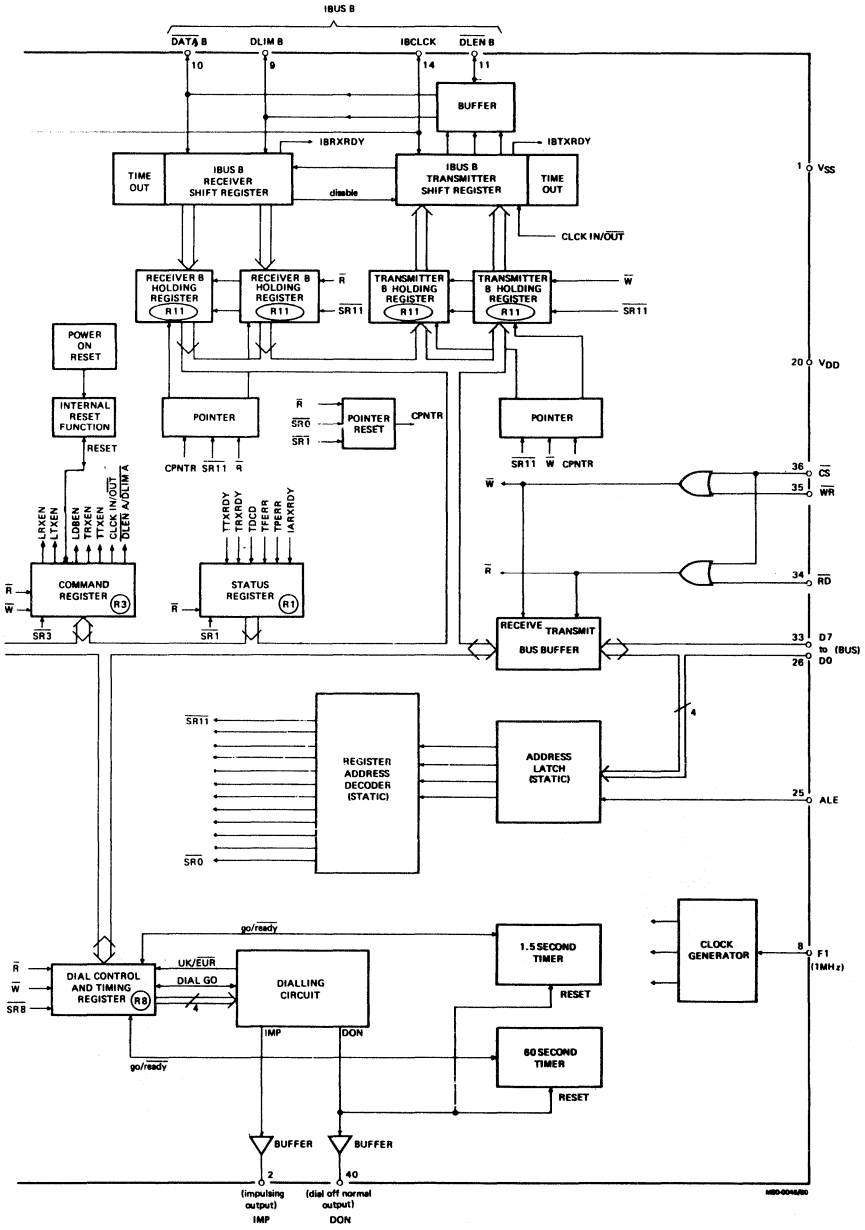


Fig. 1b. Detailed block diagram

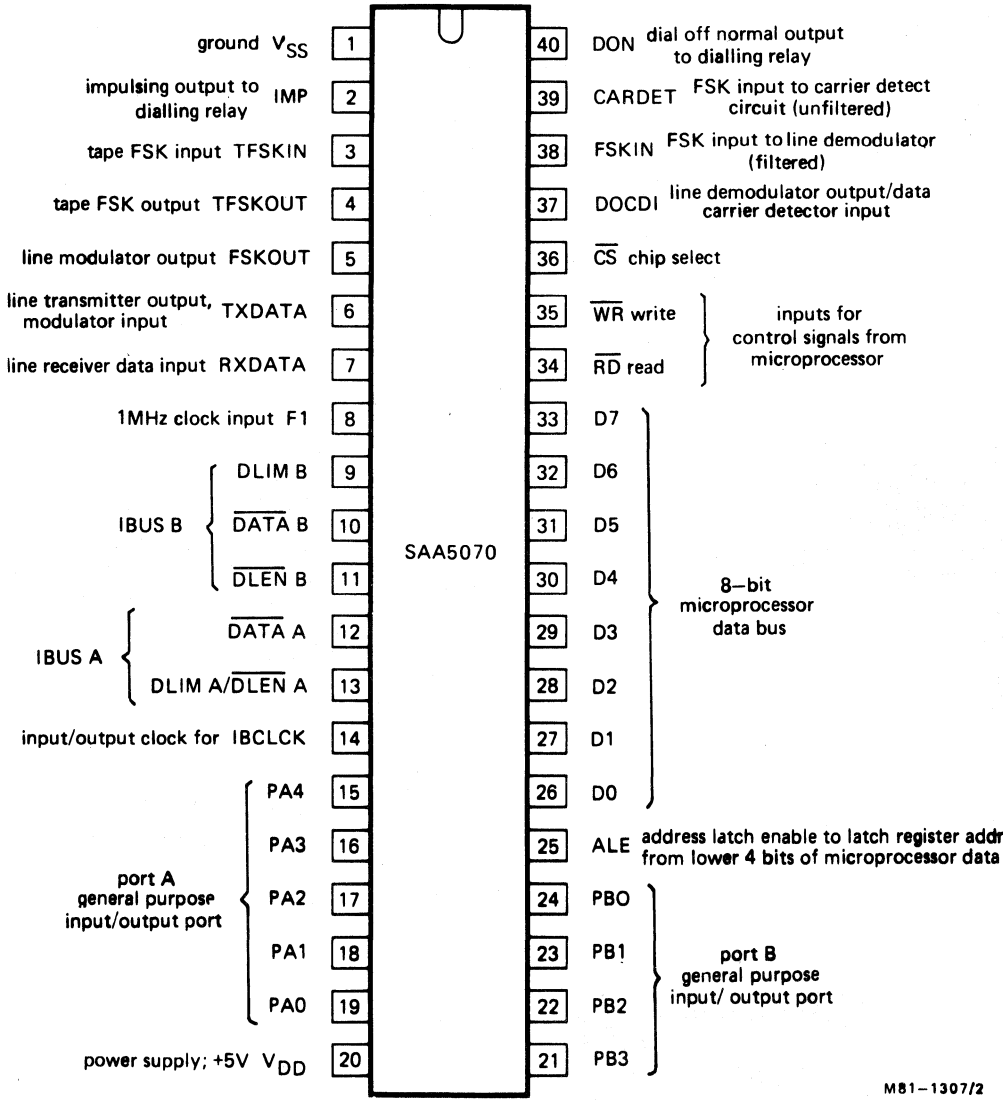


Fig.2 Pinning diagram

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all the operating frequencies. It performs most of the hardware functions of a viewdata terminal including an autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud modulator and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of pages of text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on separate ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynchronous transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an interface to a non volatile RAM which can store telephone numbers for autodialling and user passwords and Port B could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if required, in conjunction with the internal asynchronous receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter. Also the tape interface can work independently of, and simultaneously with, the line receiver.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

DEVELOPMENT DATA

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)		min.	typ.	max.	
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5	V
Input voltage:					
PORT A (pins 15 to 10) and PB0 (pin 24)	V_I	−0.3	–	14.0	V
Input voltage (all other pins)	V_I	−0.3	–	7.5	V
Temperatures					
Storage temperature range	T_{stg}			−20 to +125	°C
Operating ambient temperature range	T_{amb}			−20 to +70	°C

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150	mA
Inputs					
All inputs (except F1 clock)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

Data specific to certain inputs

		min.	typ.	max.	
F1 (1 MHz) Clock					
Input voltage; LOW	V_{IL}	−0.3	–	0.6	V
Input voltage; HIGH	V_{IH}	2.2	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Mark/space ratio (measured at 1.5 V level)		40:60	–	60:40	
$\overline{\text{DATA}}$ A, DLIM A/$\overline{\text{DLEN}}$ A (IBUS A)					
Data set up time (Fig.14)	t_{DS}	3	–	–	μs
Data hold time (Fig.14)	t_{DH}	3	–	–	μs
DLIM clock; HIGH (Fig.14)	t_{CH}	4	–	–	μs
DLIM clock; LOW (Fig.14)	t_{CL}	4	–	62	μs
Time between commands	t_{BC}	140	–	∞	μs
DLIM frequency	f_{DLIM}	16	–	160	kHz
ALE (Address Latch Enable) (Figs. 3 and 4)					
Pulse width (HIGH)	t_{ALEH}	400	–	–	ns
Cycle time	T_{ALE}	–	2500	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ (Figs. 3 and 4)					
Control pulse width	t_{WL}	–	700	–	ns
Address hold time	t_{LA}	80	–	–	ns
Address set-up time	t_{AL}	120	–	–	ns
Read cycle timings (Fig.3)					
ALE to read pulse delay time	t_{ALR}	80	–	–	ns
Read pulse (falling edge) to data bus delay time	t_{RD}	–	–	500	ns
Data hold time	t_{DR}	0	–	200	ns
Write cycle timings (Fig.4)					
ALE to write pulse delay time	t_{ALW}	80	–	–	ns
Address set-up time to $\overline{\text{WR}}$	t_{AW}	230	–	–	ns
Data set up time before $\overline{\text{WR}}$	t_{DW}	500	–	–	ns
Data hold time after $\overline{\text{WR}}$	t_{WD}	120	–	–	ns

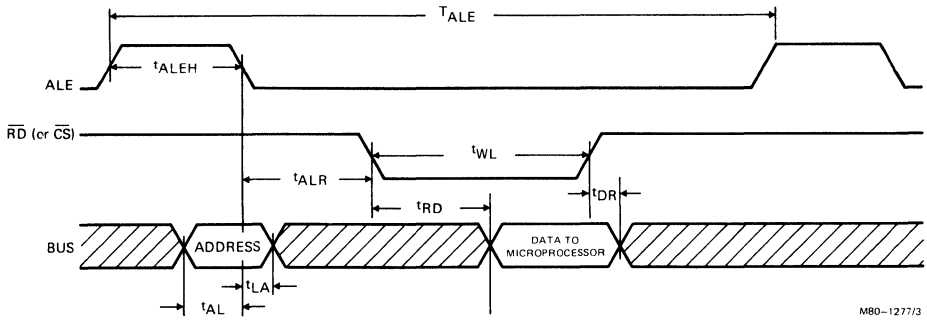


Fig.3 Read cycle timing

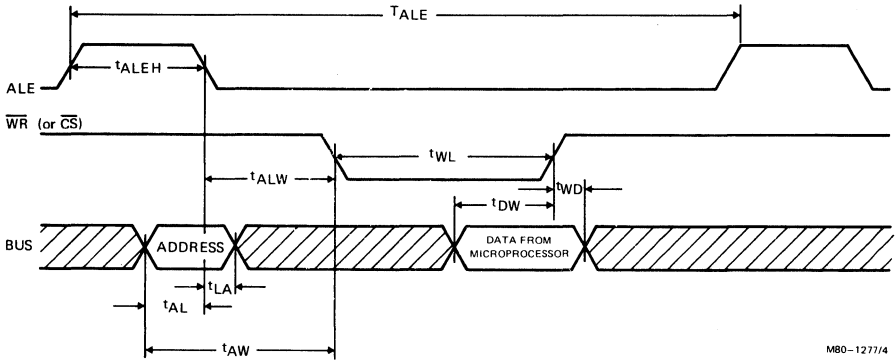


Fig.4 Write cycle timing

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

$\overline{\text{DATA}}$ B, DLIM B, $\overline{\text{DLEN}}$ B, IBCLCK (IBUS B)			min.	typ.	max.	
Input voltage; LOW	Fig.14	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r | t_f	–	–	1	μs

other timings as IBUS A

DOCDI (open drain output)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)	I_{IR}	–	0.4	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	–	V

TXDATA

(Internal resistive pull-up, permitting wired - AND connection)

Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)	$-I_{IL}$	–	–	500	μA
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)	V_{OH}	2.4	–	–	V
Load capacitance	C_L	–	–	40	pF
Output rise time (C_L = 40 pF)	t_r	–	3	–	μs

PA0 to PA4 (PORT A) (open drain output)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	13.2	V
Input capacitance	C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)	I_{OR}	–	–	10	μA
Load capacitance	C_L	–	–	40	pF
Fall time	t_f	–	–	1	μs

Inputs/Outputs (continued)		min.	typ.	max.	
PBO (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r | t_f	–	–	150	ns
Outputs					
These are protected against connection to V_{SS} or V_{DD}.					
FSKOUT and TFSKOUT					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r | t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V

Autodialling timings are given in Fig.6

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

DEVELOPMENT DATA

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.
An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 — I/O — 8-bit input/output port

Associated pins:	ALE	input	address latch enable from microprocessor
	$\overline{WR}$	input	write pulse from microprocessor
	$\overline{RD}$	input	read pulse from microprocessor
	$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: — R8 — D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins: DON output, IMP output } to drive dialling relays

Operation

The autodial section includes a clock divider, a digit impulse counter, a sequence controller and an impulse generator (see block diagram Fig.5). A sequence to generate the impulses for one digit is initiated by setting D5 (DIAL GO) to '1', D3 to D0 to the binary code of the required digit, and D7 to the required mode. This initiates the sequence controller which loads the binary code into the digit impulse counter. The counter then generates the correct number of impulses at the rate of 10 per second, together with a DON pulse which overlaps the impulses by about 7 ms at the start and end (see Figs.6, 7); the interdigit pause period is also added by the sequence controller. D5 is reset to '0' at the end of a dialling sequence and may be read by the microprocessor to determine when the dial circuit is free to accept the next digit.

D7 (UK/$\overline{\text{EUR}}$) determines the mark/space ratio of the IMP pulses

UK = 2 off to 1 on
$\overline{\text{EUR}}$ = 1.5 off to 1 on
} both one pulse per 100 ms

There is a timer in the dial circuit which can be used to time out 1.5 seconds or 60 seconds by setting D4 or D6 respectively. These bits are read/write and are reset after the relevant time out period. In addition the 60 second timer can be reset by writing a '0' to D6. The 60 second timer may be used typically by the microprocessor to release the telephone line if connection has not been made within 60 seconds. The DON pulse resets the counter so that the time out is taken from the end of the last digit dialled. Once a dialling sequence for one digit has been initiated, R8 should be used only in read mode until D5 has been reset internally to '0' indicating the end of the dial sequence for that digit.

When D5 (DIAL GO) is set to '1' the carrier detect circuit (see the next section and Fig.8) is disabled.

DEVELOPMENT DATA

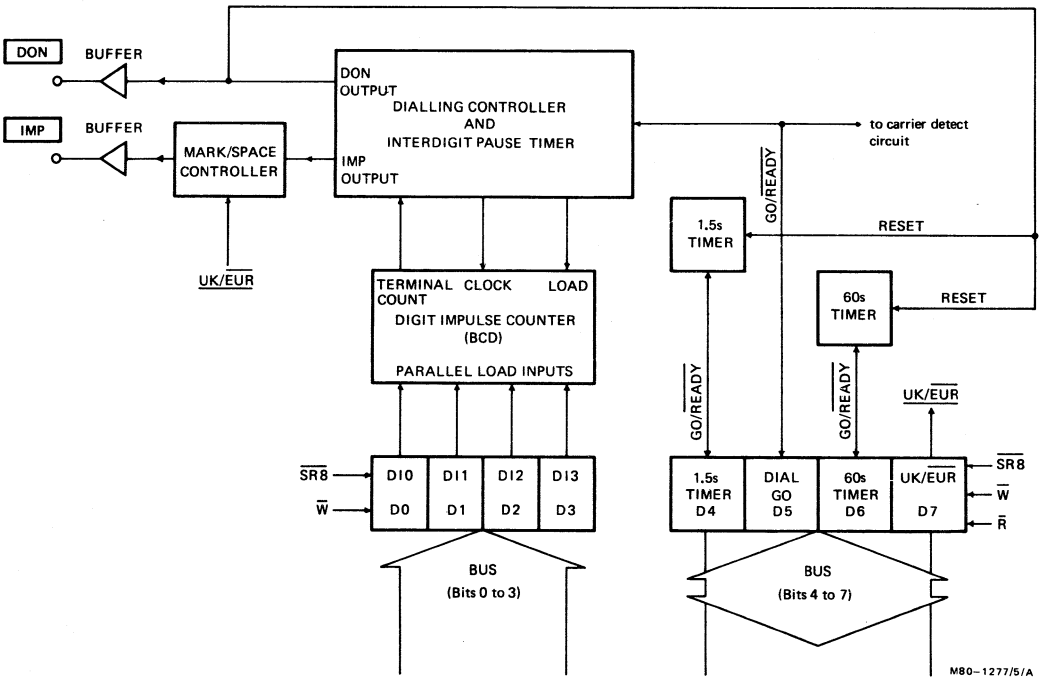
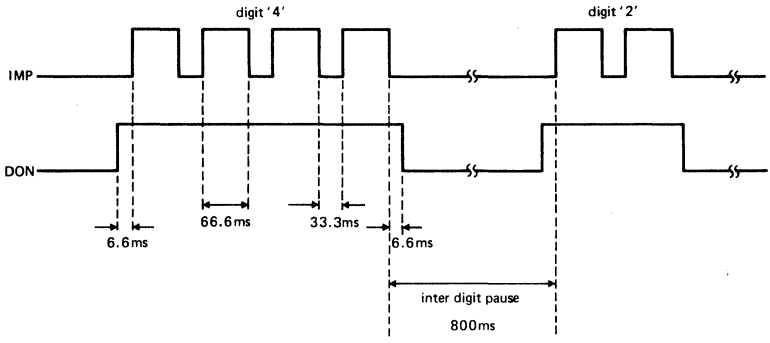


Fig.5 Autodial block diagram



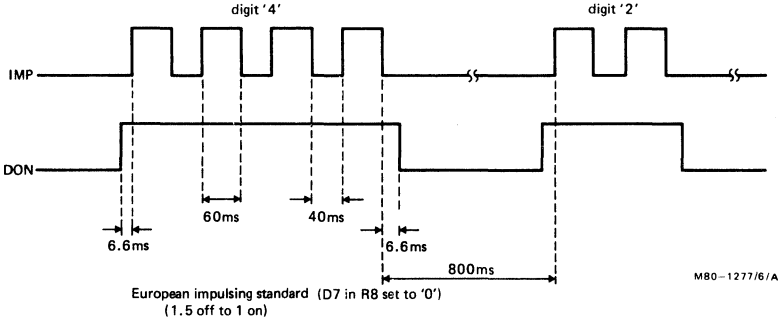


Fig.6 Autodialling timing

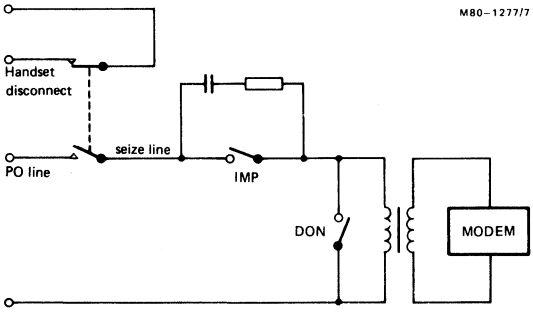


Fig.7 Simplified relay diagram

DEVELOPMENT DATA

Line Demodulator and Carrier Detect (see Fig.8)

Associated Register:– None

Associated flags in other registers:

LIDCD	–	D2	–	R0 (Status)	–	instantaneous carrier detect flag
LDCD	–	D5	–	R0 (Status)	–	carrier detect flag
$\overline{75}$/1200	–	D5	–	R2 (Mode)	–	transmit frequency baud rate (used in demodulator carrier detect circuit)
LDBEN	–	D4	–	R3 (Command)	–	line demodulator output buffer and carrier detect enable
DIAL GO	–	D5	–	R8 (Dial control)	–	used to disable carrier detect circuit during dialling sequence

Associated pins:	FSKIN	–	input	–	filtered, squared F.S.K. signal
	CARDET	–	input	–	unfiltered (squared) F.S.K. signal.
	DOCDI	–	input/output	–	demodulator output, external LDCD in

Operation

The input to the demodulator is the previously filtered and squared up F.S.K. signal from the telephone line. Its output is a pseudo analogue signal which must be externally filtered and squared to produce the demodulated data. The carrier detect circuit functions in the following modes:

a) Viewdata mode (1200 baud receive, 75 baud transmit). Initially, a narrow frequency band 'window' around 1300 Hz is accepted as carrier, this must be applied to the CARDET input. If a frequency in this range is present, the 'instantaneous carrier detected' flag will be HIGH (LIDCD), after about 2 seconds the 'line carrier detected' flag will be set HIGH (LDCD). When this occurs, the frequency window is widened to include 2100 Hz and the circuit no longer takes its input from the CARDET pin, but from the FSKIN pin.
If carrier is then removed LIDCD immediately goes LOW, and after about 1 second LDCD is reset, the frequency window again becomes narrow and around 1300 Hz and the CARDET input again becomes active. Reappearance of carrier in the 1300 Hz range will cause a repeat of the above.

b) 1200 baud each way mode
Only the instantaneous carrier detect is active in this mode. LDCD is forced LOW and the CARDET input inhibited (only FSKIN should be used in this mode).

c) External carrier detect input
If an external modem is used its (active LOW) carrier detect output is connected to DOCDI. Provided that the demodulator is not enabled, LDCD will be set if DOCDI is LOW and reset if it is HIGH.

Demodulator enable

LDCD is produced by the carrier detect circuit, which is enabled by LDBEN and disabled by DIAL GO, In the viewdata mode the demodulator is enabled by LDCD.
In the 1200 baud each way mode the demodulator is enabled directly by LDBEN.

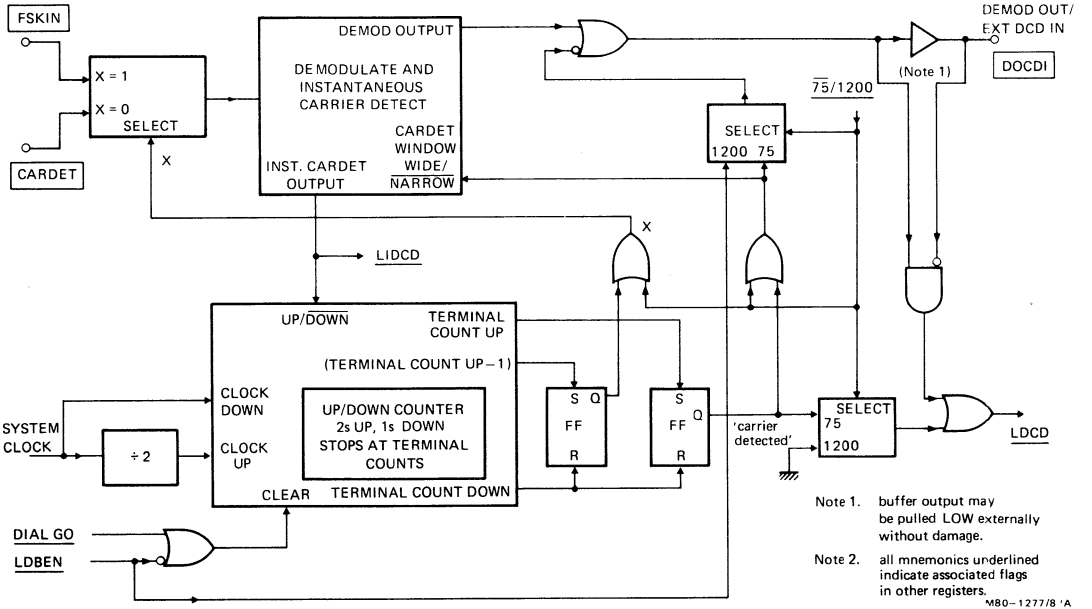


Fig.8 Line demodulator and carrier detect block diagram

Line Receiver (see Fig.9)

Associated Register: – R4 read only

Associated flags in other registers:

LRXRDY	–	D6	–	R0 (status)	–	valid data available in receive holding register
LFERR	–	D4	–	R0 (status)	–	line framing error (derived from STOP bit of message).
LPERR	–	D3	–	R0 (status)	–	line parity error.
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity detection mode select
$\overline{\text{LPEN}}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit plus parity mode select
LRXEN	–	D7	–	R3 (command)	–	line receiver enable.

Associated pins: RXDATA – input – received data input

Operation

The receiver may be configured to work with either 7 data bits and 1 parity, or with 8 data bits and no parity. Odd or even parity can be detected on chip, the LPERR flag being set when an error is detected. The required mode of operation should be selected by setting $\overline{\text{LPEN}}$ and LPO/$\overline{E}$ to the required states by writing to mode register (R2) before enabling the receiver by setting LRXEN to '1' in command register (R3). The data format is 10 bits per data word. The data word is made up of a start bit (LOW), 8 data bits, the 8th being an optional parity bit, and a stop bit (HIGH). The receive data will remain HIGH after the stop bit until the next data word. When the receiver has been enabled a negative transition is looked for on the RXDATA input indicating a possible start bit. After half a bit rate period the data is sampled again and if it is still LOW it is interpreted as a start bit, initiating a sequence which clocks the data into a shift register. When the full ten bit message has been received, the 8 data bits are parallel loaded into the receiver holding register (R4), the LRXRDY flag is set to '1'. The complement of the stop bit is loaded into the LFERR latch and the result of the parity check is loaded into LPERR latch. If line parity is not enabled i.e. $\overline{\text{LPEN}}$ = '1', then LPERR is held at '0'. The LRXRDY flag is reset to '0' after the microprocessor has read the receiver holding register (R4). The receiver has a 52 times baud rate factor to allow for maximum isochronous distortion.

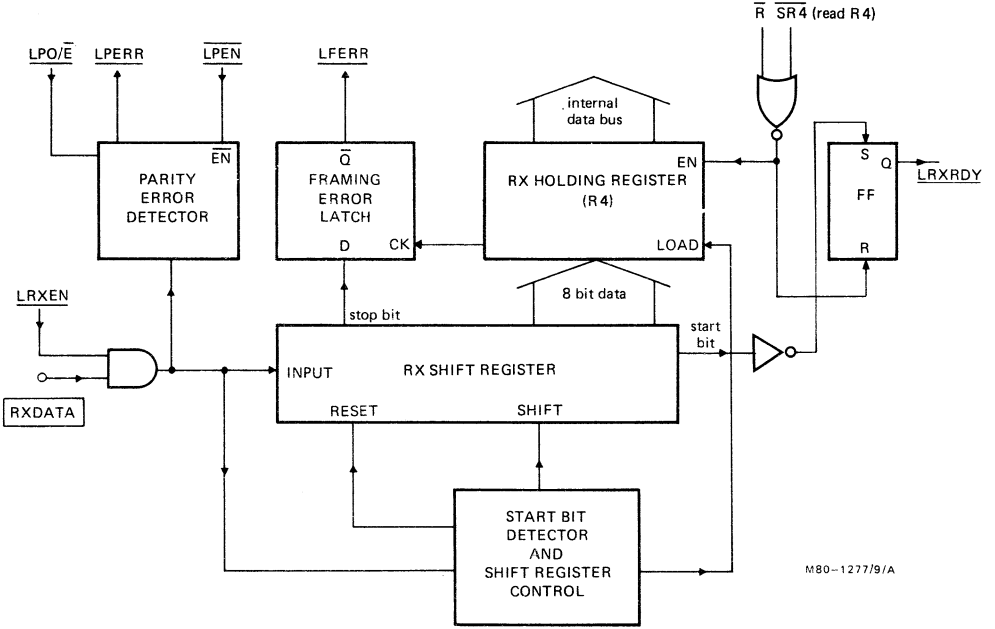


Fig.9 Line receiver block diagram

Line Transmitter (see Fig.10)

Associated Register: – R4 write only

Associated flags in other registers:

LTXRDY	–	D7	–	R0 (status)	–	transmit holding register ready to accept new data
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity mode select
$\overline{LPEN}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit data with parity mode select
$\overline{75}$/1200	–	D5	–	R2 (mode)	–	select transmit baud rate
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable

Associated pins: TXDATA – I/O – transmitter output (and also modulator input)

Operation

The data format of the transmitter is the same as that of the line receiver i.e. 10-bits, a start bit (LOW) followed by 8-data bits, the 8th bit being an optional parity (selected by LPEN), odd or even parity being selectable (by LPO/$\overline{E}$) ending with a STOP bit (HIGH) the output remaining HIGH until the next data word is written.

The transmitter and modulator may be used together or separately. The transmitter output is brought to the TXDATA pin (if LTXEN = 1) which is connected internally to the modulator input. The TXDATA pin has an internal resistive pull up permitting wire - AND connection. If the modulator is used with an off chip data source (e.g. UART) then data should not be written to the internal transmit holding register (R4). The STOP bit (HIGH) will then be continuously output when LTXEN = 1 (required to enable modulator output) allowing the external UART to control the TXDATA (pin 6).

To operate the transmitter the required mode should be set-up initially by writing to the mode register (R2) the required states of $\overline{75}$/1200, $\overline{LPEN}$, LPO/$\overline{E}$. The transmitter can then be enabled by setting LTXEN to '1' in the command register (R3). The 8-bit data word can then be written to the transmit holding register (R4). If parity is enabled then the 8th bit is ignored and the value of the parity bit calculated from the first 7-data bits and LPO/$\overline{E}$. The LTXRDY flag is set to zero when the holding register is written into. If the transmit output shift register is not currently in use the contents of the holding register are transferred to the output shift register and LTXRDY returns to '1'. This means that new data may now be written to the holding register but will not be transferred to the output shift register until the 10-bits of the current message have been clocked out. The start, stop, and parity bit (if selected) are written into the output shift register with the data word automatically.

Two transmit baud rates are selectable, 75 baud for viewdata transmissions or 1200 baud for private data communication systems.

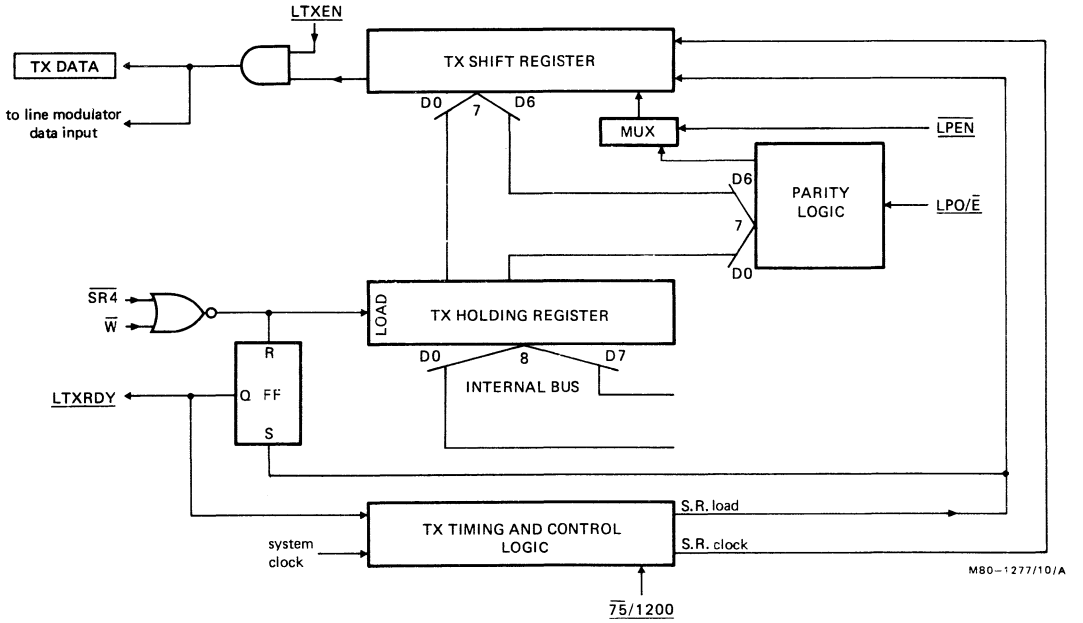


Fig.10 Line transmitter block diagram

Line Modulator (see Fig.11)

Associated Register: – None

Associated flags in other registers:

$\overline{75}$/1200	–	D5	–	R2 (mode)	–	transmit baud rate select.
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable.

Associated Pins:	TXDATA	–	I/O	–	modulator input (also (on chip) transmitter output).
	FSKOUT	–	output	–	line modulator output

Operation

The modulator generates a pseudo analogue signal from a serial shift register which is parallel loaded with patterns from an internal ROM. The frequency of the sine wave is determined by the selected baud rate $\overline{75}$/1200, and the value of the data on TXDATA (pin 6).

data	'1'	'0'
1200 baud	1300 Hz	2100 Hz
75 baud	390 Hz	450 Hz

One sine wave cycle is comprised of a 92-bit pattern which after minimal external low pass filtering provides a suitable F.S.K. signal out (see Fig.11)

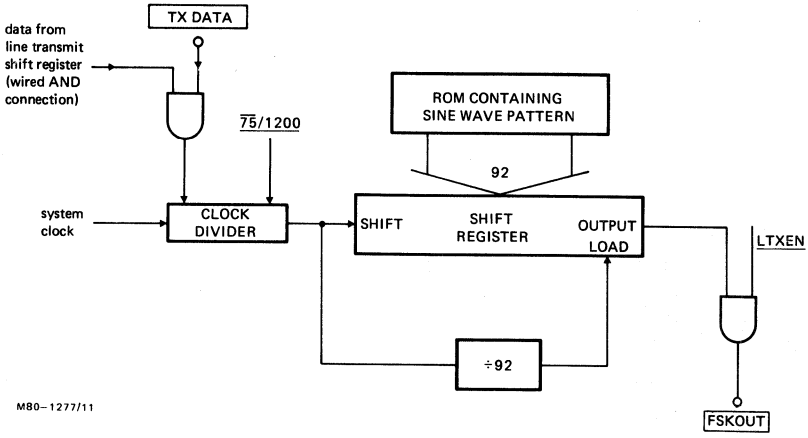


Fig.11 Line modulator block diagram

Tape section (see Fig.12)

Associated registers: – R5 – Consists of two registers with the same address:
transmit holding register write only
receive holding register read only

Associated flags in other registers:

TTXRDY	–	D7	–	R1 (status)	–	transmit holding register ready to accept new data
TRXRDY	–	D6	–	R1 (status)	–	valid data available in receive holding register
TDCD	–	D5	–	R1 (status)	–	tape data carrier detect flag
TFERR	–	D4	–	R1 (status)	–	tape framing error (derived from STOP bit of message)
TPERR	–	D3	–	R1 (status)	–	tape parity error
TPO/$\overline{E}$	–	D3	–	R2 (mode)	–	odd or even parity mode select.
$\overline{TPEN}$	–	D2	–	R2 (mode)	–	8-bit data or 7-bit plus parity mode select
TRXEN	–	D3	–	R3 (command)	–	tape receiver enable
TTXEN	–	D2	–	R3 (command)	–	tape transmitter enable

Associated pins:	TFSKIN	– input	–	F.S.K. input to tape sections
	TFSKOUT	– output	–	F.S.K. modulated data out

DEVELOPMENT DATA

Operation of tape section (see Fig.12)

The tape data modulation system is a modified form of the 'Kansas City' standard. A logic '1' is represented by one cycle of 1300 Hz, and a logic '0' by two cycles of 2600 Hz, the data rate being 1300 baud. The data format is the same as that for viewdata, i.e. 10-bit words consisting of a START bit (LOW), followed by 8-data bits, the 8th being an optional parity bit, ending with a STOP bit (HIGH) which is continuous until the next data word.

To operate the tape section the required parity mode should first be set up by writing the required states of TPEN and TPO/$\overline{E}$ to the mode register (R2). The TTXEN command enables the output of the transmit shift register into the modulator, and should be set before data is written to the transmit holding register. (With TTXEN = '0' the modulator outputs a continuous 1300 Hz signal '1'). When a data word is written to the transmit holding register the TTXRDY flag is reset to '0'. If the transmit shift register is not currently active the contents of the holding register, along with valid parity bit (if enabled) and the START and STOP bits are transferred to the transmit shift register, at the same time TTXRDY is set to '1'. The holding register is then free to accept new data but this will not be transferred to the shift register until the current data has been clocked out. Data should be written to the tape transmit holding register, therefore, only when TTXRDY = '1'.

The modulator produces 1300 Hz and 2600 Hz signals which occur synchronously with the data from the transmitter. Hence a '1' is one complete 1300 Hz cycle, and a '0' two complete 2600 Hz cycles. The modulator output, TFSKOUT, requires minimal external low pass filtering to produce data suitable for audio cassette tape recorders.

To overcome the tendency of cassette recorders to attenuate high frequencies, the 1300 Hz signal contains 2 μs wide attenuating pulses every 12 μs. This reduces the 1300 Hz signal by approximately 3 dB relative to the 2600 Hz signal after external filtering.

The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred simultaneously (via the microprocessor) to tape.

The TFSKIN input accepts the previously filtered and squared data from the tape recorder. The demodulator uses the fact that the modulated data is in phase with clock to regenerate the clock from the data. This permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag to '1' if carrier (1300 Hz or 2600 Hz) is valid for 100 ms. If carrier is lost for 100 ms the TDCD flag is reset to '0'. This flag may be read by the microprocessor to determine when to enable the tape receiver by setting TRXEN to '1'.

If TRXEN is set, then on detection of a start bit (LOW) data is shifted into the tape receive shift register by the clock which has been extracted from the data. After ten clocks, the contents of the shift register are transferred to the receive holding register. At the same time the complement of the STOP bit is loaded into the TFERR latch, the results of the parity calculation loaded into the TPERR latch, and TRXRDY is set to '1'. The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register and is reset to '0' when the holding register (R5) is read.

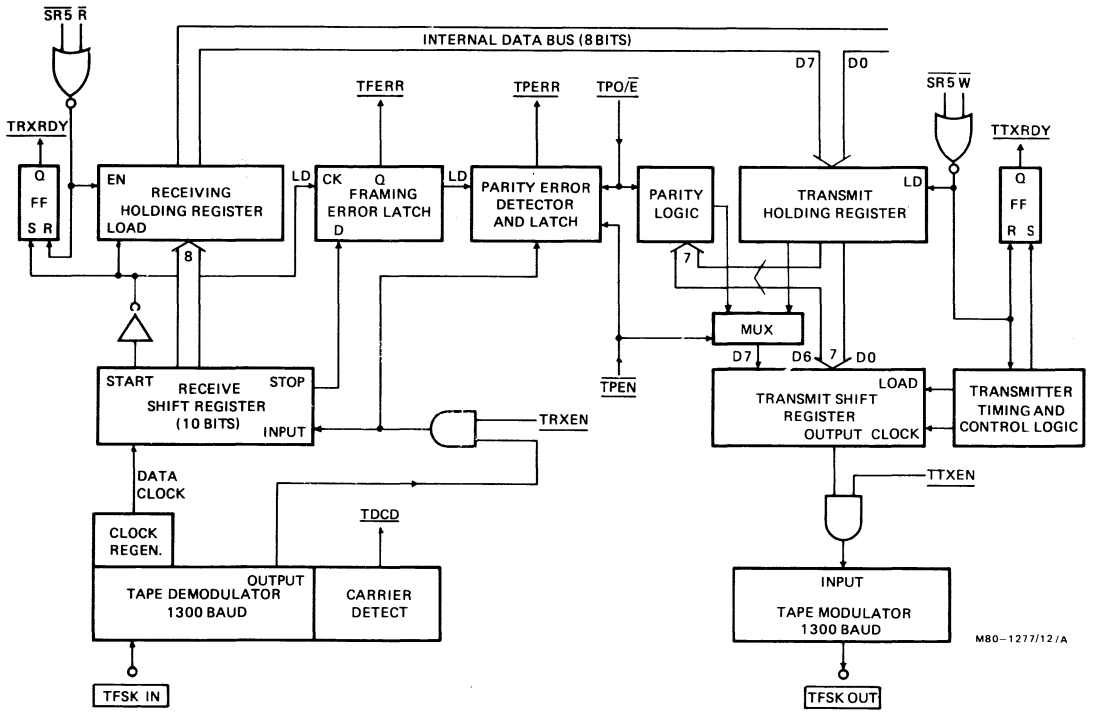


Fig.12 Tape section block diagram

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes)	–	R10	–	read only
Receiver B (2 bytes)	–	R11	–	read only
Transmitter B (2 bytes)	–	R11	–	write only

Associated flags in other registers:

IBRXRDY	–	D1	–	R0 (status)	–	valid data available in receiver B holding register
IBTXRDY	–	D0	–	R0 (status)	–	transmitter B holding register ready to accept new data
IARXRDY	–	D1	–	R1 (status)	–	valid data available in receiver A holding register
CLCK IN/$\overline{\text{OUT}}$	–	D1	–	R3 (command)	–	input/output control for 62.5 kHz pin
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	–	D0	–	R3 (command)	–	3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{\text{DATA}}$ A	– input	–	receiver A data input
DLIM A/$\overline{\text{DLEN}}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{\text{DATA}}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{\text{DLEN}}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

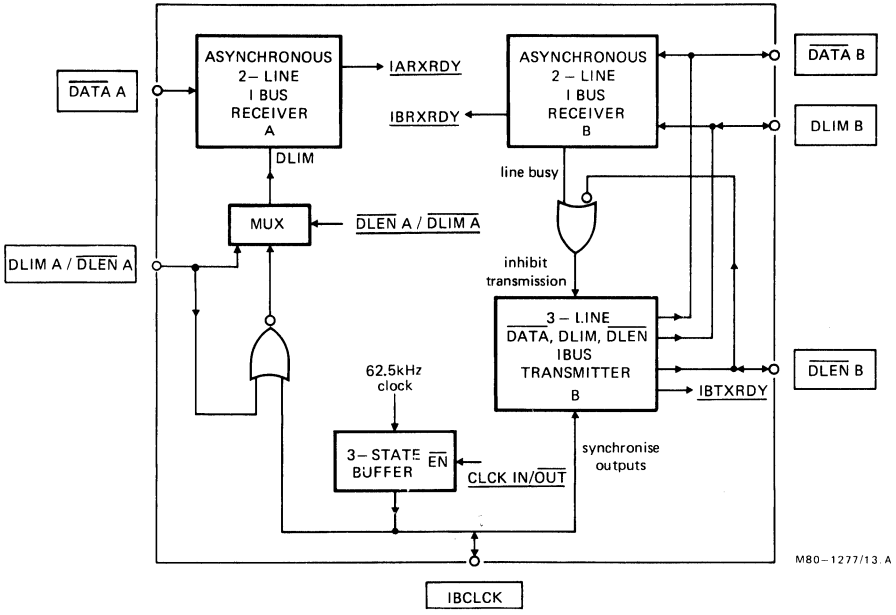


Fig.13 IBUS block diagram

For the transmitter the register pair is organised as:

	D7	D6	D5	D4	D3	D2	D1	D0
1st byte TXB – R11A	8	7	6	5	4	3	2	1

	D7	D6	D5	D4	D3	D2	D1	D0
2nd byte TXB – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

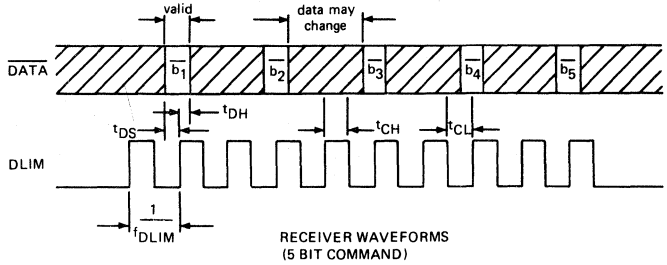
Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

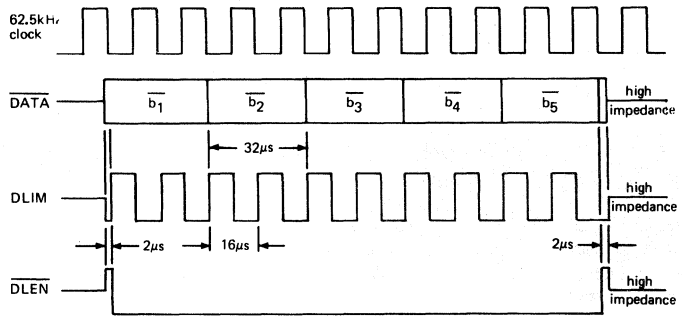
Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM). Receiver B is inhibited from receiving data transmitted by transmitter B.

Receiver A may operated either as a two line receiver with $\overline{\text{DATA}}$ and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and CLK receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A command D0, register R3 (command).

The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The function is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3



RECEIVER WAVEFORMS
(5 BIT COMMAND)



TRANSMITTER WAVEFORMS
(5 BIT COMMAND)

MBO-0045/65

Fig. 14 IBUS waveforms

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 5 V. PB0 is open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LDCD R	LFERR R	LPERR R	LIDCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TDCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{\text{LPEN}}$ R/W	$\overline{75}$/1200 R/W		TPO/$\overline{E}$ R/W	$\overline{\text{TPEN}}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LDBEN R/W	TRXEN R/W	TTXEN R/W	CLCK IN/$\overline{\text{OUT}}$ R/W	$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{\text{EUR}}$ R/W	60s TIMER R/W	DIAL GO R/W	1.5s TIMER R/W	DI 3 W	DI 2 W	DI 1 W	DI 0 W	DIAL CONTROL AND TIMING REGISTER
R10 A	B8 R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	IBUS A REGISTERS
R10 B	– WL3 R	– WL2 R	– WL1 R	– WL0 R	– B12 R	– B11 R	– B10 R	– B9 R	

APPENDIX

Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
	—	—	—	—	—	—	—	—	
R11 B	WL3 R/W	WL2 R/W	WL1 R/W	WL0 R/W	B12 R/W	B11 R/W	B10 R/W	B9 R/W	

NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready – data available
IBRXRDY	IBUS B receiver ready – data available
IBTXRDY	IBUS B transmitter ready – previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error – received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready – data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready – transmit holding register empty
$\overline{\text{SR}}$n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error – received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready – data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready – transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register