TELETEXT VIDEO PROCESSOR

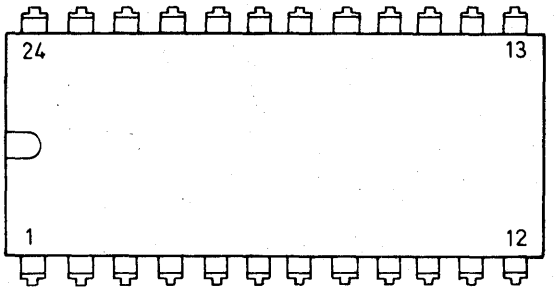
The SAA5030 is a monlithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext TV data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{supply}	nom	12	V
Supply current at V_{supply} = 12 V	I_{supply}	typ	110	mA
Video input amplitude (sync-white)	$V_{16\,video(p\text{-}p)}$	nom	2.4	V
Teletext data input amplitude	$V_{16\,teletext(p\text{-}p)}$	nom	1.1	V
Sync amplitude	$V_{16\,sync(p\text{-}p)}$	nom	0.7	V
Operating temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101 with heat spreader)



Viewed from top

PINNING

1. Signal presence time constant components.
2. Line reset time constant
3. Fast line reset output (FLR)
4. Ground (0V)
5. Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)
6. 6 MHz output (F6)
7. Phase detector time constant components
8. 6 MHz crystal
9. 6 MHz crystal
10. Picture on input (PO)
11. After hours sync input ($\overline{AHS}$)
12. Sync output to TV
13. Field sync output (FS)
14. Field sync separator timing.
15. Sync separator capacitor
16. Composite video input
17. Supply voltage (+ve)
18. Clock output (F7)
19. $\overline{Data}$ output
20. Clock phase adjustment
21. Clock regenerator coil
22. Clock pulse timing capacitor
23. Peak detector capacitors
24. Peak detector capacitors

RATINGS Limiting values in accordance with the Absolute Maximum System.

Voltages					
Supply voltage	V_{17-4}	V_{supply}	max.	13.2	V
Input voltages	V_{5-4}	V_{in}	max.	9.0	V
	V_{10-4}	V_{in}	max.	V_{supply}	V
	V_{11-4}	V_{in}	max.	7.5	V
Dissipation				t.b.f.	W
Temperatures					
Storage temperature		T_{stg}		−20 to +125	°C
Operating ambient temperature		T_{amb}		−20 to +70	°C

CHARACTERISTICS (At T_{amb} = 25 °C, V_{supply} = 12 V and with external components as shown in Fig.1 unless otherwise stated)

			min.	typ.	max.	
Supply voltage	V_{17-4}	V_{supply}	10.8	12.0	13.2	V
Supply current (V_{supply} = 12.0 V)		I_{supply}	–	110	–	mA
Video input and sync separator						
Video input amplitude (sync to white) Fig.2		$V_{16\,video(p-p)}$	2.0	2.4	3.0	V
Source impedance, f = 100 kHz		Z_s	–	–	250	Ω
Sync amplitude		$V_{16\,sync(p-p)}$	0.07	0.7	1.0	V
Delay through sync separator			–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.3)			32	48	62	μs
Field sync output						
V_{out} (low) at I_{13} = +20 μA		V_{13L}	–	–	0.5	V
V_{out} (high) at I_{13} = −100 μA		V_{13H}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue no. 4322 143 03241

C_1 = 27.5 fF (typ)

C_0 = 6.8 pF (typ)

C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz

Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	F6	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, V_{9-8} measured with input voltage of 100 mV(p-p) and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load		–	–	30	ns

Data slicer and clock regenerator

Teletext data input amplitude, pin 16 (Note 2, Fig. 2); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop (peak-to-peak value)		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16					
	Positive	–	15	–	V/μs
	Negative	–	9	–	V/μs
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	–	ns

Data slicer and clock regenerator (continued)	min.	typ.	max.	
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)	20	–		Clock Periods
Data and clock output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value	–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	–	–	30	ns
Input voltage for energising clock phase setting circuit, pin 10	10	–	–	V
Sandcastle input				
Sandcastle detector thresholds, pin 5				
Phase lock pulse ($\overline{PL}$) on	2	–	–	V
Phase lock pulse off	–	–	3	V
Blanking pulse ($\overline{CBB}$) on	4.5	–	–	V
Blanking pulse off	–	–	5.5	V
Dual polarity sync buffer				
After hours sync ($\overline{AHS}$) pulse input pin 11				
Threshold for $\overline{AHS}$ active	1.0	–	–	V
Threshold for $\overline{AHS}$ off	–	–	2.0	V
Picture on (PO) input, pin 10				
Threshold for PO active	–	–	2.0	V
Threshold for PO off	1.0	–	–	V
Sync output, pin 12				
AHS output with pin 10 < 1 V (Note 5); peak-to-peak value	–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value	–	0.7	1.0	V
Output current	–	–	3	mA
Line reset and signal presence detectors				
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)	–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)	–	7.8	–	V
Line reset output V_{out} (low) at $I_3 = +20\ \mu A$	–	–	0.5	V
Line reset output V_{out} (high) at $I_3 = -100\ \mu A$	2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal	–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected	–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14 bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative going centred on +9.7 V.
6. When composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** 0V

5. **Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. PL is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of PL are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8,9 **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture on input (PO)**

The PO signal from the acquisition and control circuit SAA5040 is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the TV (see pin 10).

12. **Sync output to TV**

Either the input video or $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is high or low. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage + 12 V**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuit SAA5040 via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuit SAA5040 via a series capacitor.

→ 20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuit SAA5040 via pin 18.

23,24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video. Storage capacitors are connected to these pins for the negative and positive peak detectors.

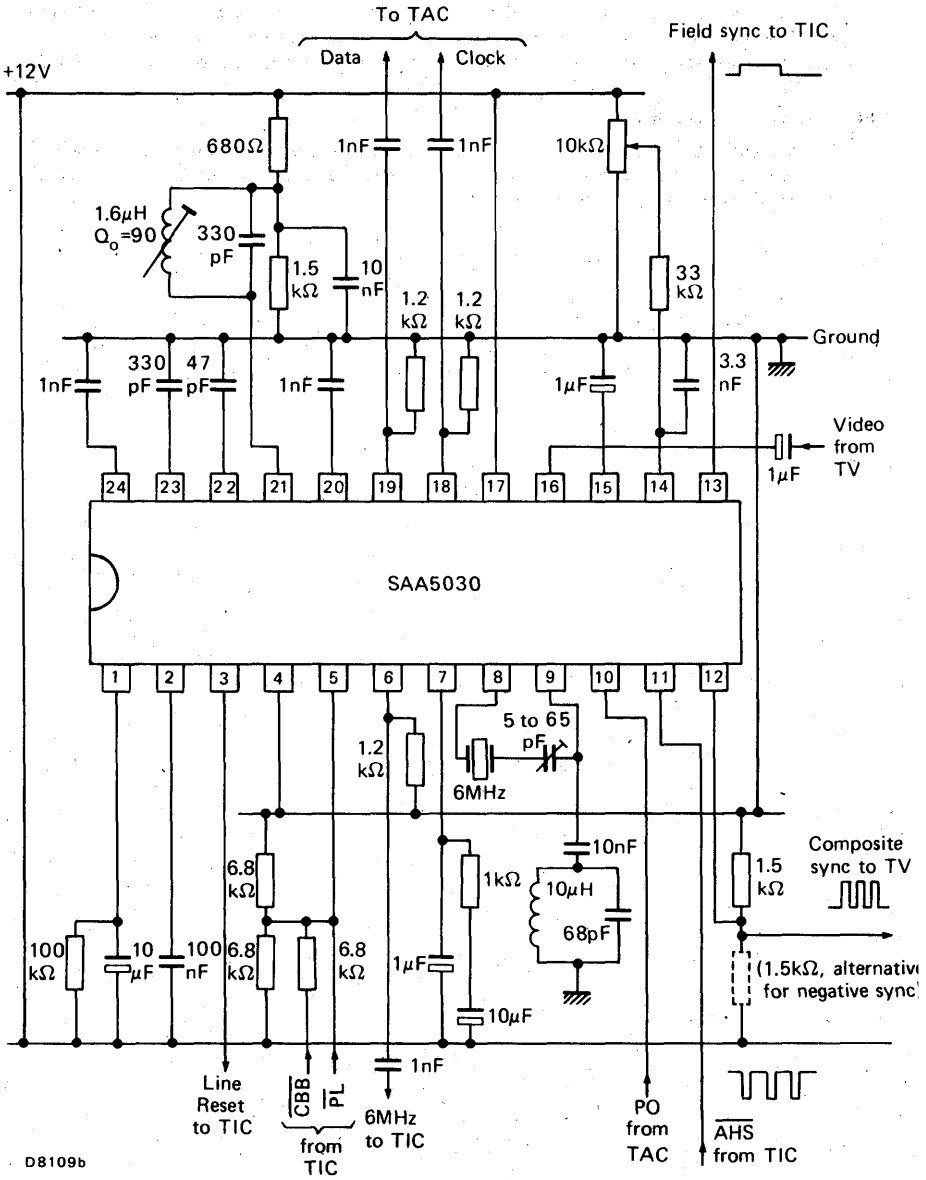


Fig.1 Peripheral circuit.

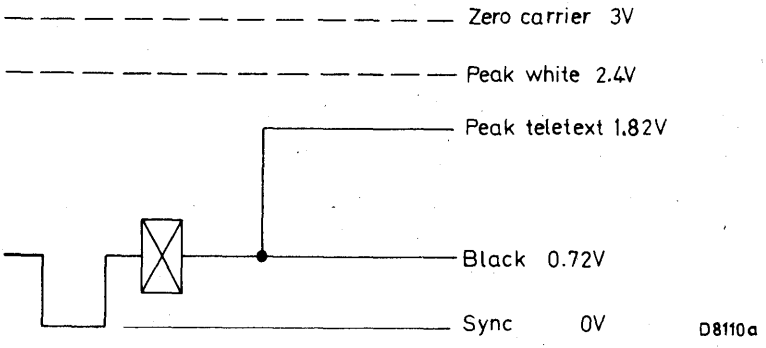


Fig. 2 Part of teletext line, with burst, showing nominal levels.

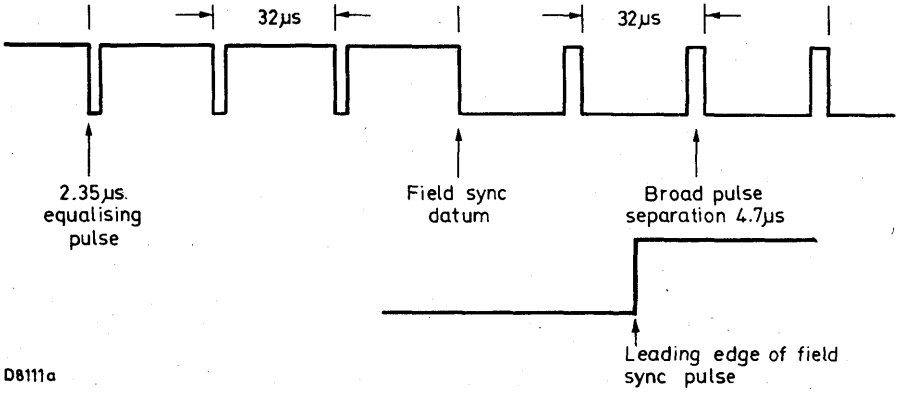


Fig. 3 Detail of idealised composite sync waveform.