DISPLAY INTERFACE AND FREQUENCY COUNTER

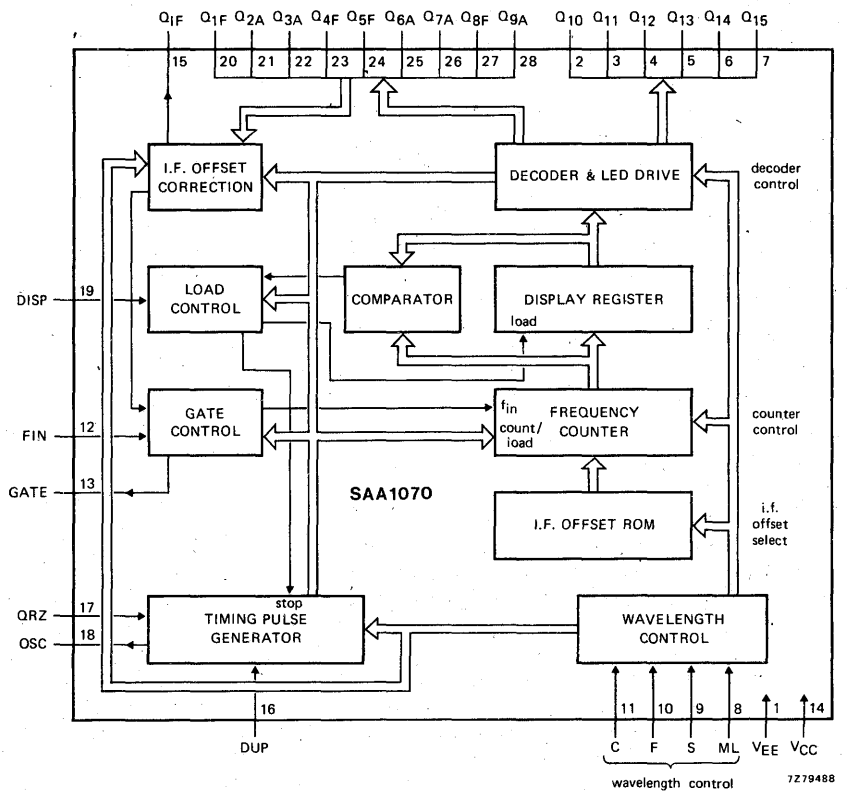


Fig. 1 Block diagram.

Features

- 18-bit frequency counter, 4½-digit LED driver and decoder.
- Internal timing unit with an external 4 MHz quartz crystal.
- 16-bit comparator eliminating the influence of interferences and display flicker.
- Display test and blanking facilities.
- A wide range of i.f. offset frequencies programmable by the user.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,5 to 5,5 V
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Input frequency	f_I	<	3,75 MHz
Output current at V_Q = 0,5 V	I_Q	<	60 mA
Supply current	I_{CC}	typ.	90 mA

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

GENERAL DESCRIPTION

A frequency indicator system can be made with the SAA1070 and the frequency divider SAA1058. It has the following features:

- A 4½-digit LED display driver. Action starts in duplex mode: the indicators are driven by half sine-wave pulses, the two character groups are switched during the zero crossing of the duplex phases. This will obtain minimum interference at correct exploitation of the terminals.
- An 18-bit frequency counter with display decoder and indicator memory. The counter can be preset in a wide range of programmed offset frequencies, so it is possible to obtain, independent of each other, 15/24 different i.f. signals in the FM, SW, MW and LW ranges.
- A timing unit driven by a 4 MHz quartz crystal on the chip.
- A 16-bit comparator for loading the measured frequencies. The frequency value in the display latch will only be changed when three successive counter values are different to the latch values. This eliminates display flicker for interferences and reduces the sensibility.
- Latch loading; in this case the frequency counter and the prescaler are stopped and the last measured frequency is displayed continuously.
- In FM operation choice of displaying received frequency or channel number.
- Display test and blanking facilities.

OPERATION DESCRIPTION

The timing for a measurement cycle is started at a positive-to-negative transition of input DUP (pin 16). The internal timing unit generates pulses of different length in which the programmed i.f. signals will be determined (see Tables 1 and 2). During this time the driver outputs Q_1 to Q_9 are internally switched as inputs; the driver outputs are blocked. The programming of a '1' or '0' is achieved by using or omitting 22 kΩ resistors between the appropriate output and pin 15 (Q_{IF}), or between these outputs and + 2,5 V (see Fig. 4).

The counter is preset (parallel i.f. presetting) depending on the i.f. chosen and the mode of operation (FM, SW, MW and LW, see Table 3). This is followed by serial offset; the counter then has a pulse train applied via a gating circuit, the number of pulses also depends on the programming of Q_1 to Q_9 and the mode of operation. The gating circuit releases input FIN (pin 12) for a defined time, in which the applied pulse to FIN switches the counter.

A HIGH level is obtained at output GATE (pin 13) during this specified measuring time; after that the 16 most significant bits of the counter will be compared with the contents of the latch. If an unequal content is detected a 2-bit comparator counter is incremented: an equal state of the comparator resets this counter. As soon as the comparator counter is in position 3, i.e. after three successive different counter values, the new counter contents will be transferred to the latch at the following positive-to-negative transition of signal DUP. The latch value will be decoded for a 7-segment display and transferred to the LED outputs Q_1 to Q_{15} via a duplex circuit. The LED segments have to be connected to the display outputs via current-limiting resistors (as explained above).

Table 1. Setting of i.f. offset frequencies for FM operation.
Wavelength control: WLC = F.C.

pin number				offset frequency
27	24	23	20	MHz
0	0	0	0	10,7000
0	0	0	1	10,6000
0	0	1	0	10,6125
0	0	1	1	10,6250
0	1	0	0	10,6375
0	1	0	1	10,6500
0	1	1	0	10,6625
0	1	1	1	10,6750
1	0	0	0	10,6875
1	0	0	1	10,7000
1	0	1	0	10,7125
1	0	1	1	10,7250
1	1	0	0	10,7375
1	1	0	1	10,7500
1	1	1	0	10,7625
1	1	1	1	10,7750

Table 2. Setting of i.f. offset frequencies for AM operation.
Wavelength control: WLC = S.ML.

pin number					offset frequency kHz	
28	26	25	22	21	S	ML
0	0	0	0	0	460,00	460
0	1	0	0	0	448,75	449
0	1	0	0	1	450,00	450
0	1	0	1	0	451,25	451
0	1	0	1	1	452,50	452
0	1	1	0	0	453,75	453
0	1	1	0	1	455,00	454
0	1	1	1	0	456,25	455
0	1	1	1	1	457,50	456
1	0	0	0	0	456,25	457
1	0	0	0	1	457,50	458
1	0	0	1	0	458,75	459
1	0	0	1	1	460,00	460
1	0	1	0	0	461,25	461
1	0	1	0	1	462,50	462
1	0	1	1	0	463,75	463
1	0	1	1	1	465,00	464
1	1	0	0	0	463,75	465
1	1	0	0	1	465,00	466
1	1	0	1	0	466,25	467
1	1	0	1	1	467,50	468
1	1	1	0	0	468,75	469
1	1	1	0	1	470,00	470
1	1	1	1	0	471,25	471
1	1	1	1	1	472,50	472

0 = no resistor.
1 = 22 kΩ resistor to + 2,5 V (see Fig. 4).

OPERATION DESCRIPTION (continued)

The operation mode of the circuit depends on the state of the wavelength control inputs (pins 8 to 11); see Table 3.

Table 3. Truth table of the WLC inputs.

operation mode	wavelength control inputs F | C | S | ML pin number 10 | 11 | 9 | 8			
v.h.f. frequency (FM)	0	1	1	1
v.h.f. channel (FM)	X	0	1	1
short wave	1	X	0	1
medium wave	1	X	1	0
long wave	1	X	1	0
display test	0	0	1	0
display blanking	0	X	0	X
display blanking	1	X	0	0
display blanking	0	1	1	0
display blanking	1	1	1	1

0 = 0 V (ground)
1 = +5 V
X = state is immaterial

The display position and resolution of the frequency measurement is given in Table 4.

Table 4.

operation mode	display range (number of indicators) min. 1	2	3	4	5	max. 1	2	3	4	5		resolution
v.h.f. frequency (FM)		0	0	0	0	1	9	9	9	5*	MHz	0,05 MHz
v.h.f. channel (FM) ▲	–		0	0		+		9	9	**		0,1 MHz
short wave		0	0	0	0	1	9	9	9	5	kHz	5,0 kHz
medium/long wave		0	0	0		1	9	9	9		kHz	1,0 kHz

* Limited to 109,30 MHz for a maximum input frequency of 3,75 MHz.
** Limited to −64 for a maximum input frequency of 3,75 MHz.
▲ One channel = 300 kHz; e.g. channel 02 = 87,6 MHz

The display frequency corresponds to the frequency to be measured, at an input frequency f_{in} at pin 12:

$$f_{in} = \frac{f_m + f_{offset}}{32}$$

in which: f_{in} = input frequency,
f_m = frequency to be measured,
f_{offset} = i.f. offset frequency programmed as is Tables 1 and 2.

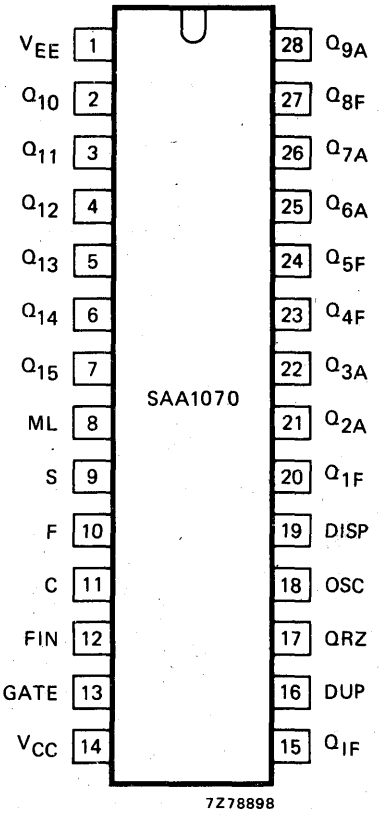


Fig. 2 Pinning diagram.

PINNING

14	V_{CC}	positive supply
1	V_{EE}	negative supply (0 V, ground)

Inputs

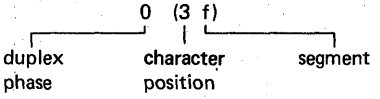
8	ML	medium and long wave } wavelength control; when connected to ground
9	S	short wave } wavelength control; when connected to ground
10	F	FM } wavelength control; when connected to ground
11	C	channel control when connected to ground; other functions can be obtained by connecting more wavelength control inputs to ground simultaneously (see Table 3).
12	FIN	input for frequency to be measured
16	DUP	synchronization of the internal timing unit and selection of the character groups (duplex input)
17	QRZ	input for the quartz-crystal oscillator

PINNING (continued)

19	DISP	control input for mode of operation open: comparator operates grounded: stop display is obtained; the timing unit is stopped in position 20 and cannot be started again by the duplex input (DUP); the last displayed value remains stored in the latches and is driven to the output; the comparator counter is reset; output GATE (pin 13) is LOW at V_{CC}: the comparator function is switched-off; the contents of the counter are loaded into the latches every period 18 of the timing unit; the timing unit will also be stopped at the beginning of period 17 independent of the state of the comparator output; in that case the display rate will be higher

Inputs/outputs

The following notation is used for the LED driver outputs:



e.g. 1 (4a) means: on duplex input = 1; the 'a' segment of the fourth digit is driven.

20	Q_{1F}	LED output 0 (3f); 1 (2f) i.f. offset input 1 for FM
21	Q_{2A}	LED output 0 (3g); 1 (2g) i.f. offset input 1 for AM
22	Q_{3A}	LED output 0 (3e); 1 (2e) i.f. offset input 2 for AM
23	Q_{4F}	LED output 0 (3d); 1 (2d) i.f. offset input 2 for FM
24	Q_{5F}	LED output 0 (3c); 1 (2c) i.f. offset input 3 for FM
25	Q_{6A}	LED output 0 (3b); 1 (2b) i.f. offset input 3 for AM
26	Q_{7A}	LED output 0 (3a); 1 (2a) i.f. offset input 4 for AM
27	Q_{8F}	LED output 0 (5g); 1 (4b) i.f. offset input 4 for FM
28	Q_{9A}	LED output 0 (1d); 1 (4f) i.f. offset input 5 for AM

Outputs

2	Q_{10}	LED output 0 (5a, 5d); 1 (4a)
3	Q_{11}	LED output 0 (5b, 5e); 1 (4c)
4	Q_{12}	LED output 0 (5c, 5f); 1 (4d)
5	Q_{13}	LED output 0 (1c); 1 (4g)
6	Q_{14}	LED output 0 (1a, 1b); 1 (4e)
7	Q_{15}	LED output 0 (3h, MHz indicator); 1 (kHz indicator)
15	Q_{IF}	i.f. offset control output; this output is set to 2,5 V at the beginning of a measuring period; when programming resistors are connected to this pin, it must also be connected to both phases of the LED anode voltages via diodes; this prevents a segment being switched off by the programming resistors.
13	GATE	open collector output; counter is active when this pin is HIGH; also used to drive the reset input of the divide by 32 prescaler (SAA1058)
18	OSC	output for the quartz-crystal oscillator

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,5 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.	
Supply voltage	V_{CC}	4,5	5	5,5	V
Supply current	I_{CC}	–	90	–	mA
Inputs ML, S, F, C					
open voltage	V_{IO}	2,5	4,5	–	V
input voltage HIGH	V_{IH}	2,0	–	5,0	V
input voltage LOW	V_{IL}	0	–	1,0	V
input current LOW; V_{IL} = 1 V	$-I_{IL}$	30	–	300	μA
Input DUP					
input voltage HIGH	V_{IH}	1,0	–	12,0	V
input voltage LOW	V_{IL}	−6,0	–	0,4	V
input resistance HIGH	R_{IH}	0,6	–	1,5	kΩ
Input FIN					
input voltage HIGH	V_{IH}	2	–	5	V
input voltage LOW	V_{IL}	0	–	1	V
input current HIGH	I_{IH}	–	–	20	μA
input capacitance	C_I	–	–	4	pF
input frequency	f_I	–	–	3,75	MHz
Inputs Q_{1F}, Q_{2A}, Q_{3A}, Q_{4F}, Q_{5F}, Q_{6A}, Q_{7A}, Q_{8F}, Q_{9A}					
input voltage HIGH	V_{IH}	1,8	–	12	V
open voltage (logic LOW)	V_{IO}	0,2	1,4	1,5	V
input current HIGH	I_{IH}	10	20	30	μA
programming resistor between input and pin 15 (at 2,5 V for HIGH)	R_{IF}	15	22	33	kΩ
I.F. offset					
accuracy; WLC = F.C.		–	–	± 8	kHz
accuracy; WLC = S.M.L.		–	–	± 0,6	kHz
supply sensitivity; WLC = F.C.		–	–	10	kHz/V
supply sensitivity; WLC = S.M.L.		–	–	0,8	kHz/V

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	
Input DISP					
open voltage HIGH } note 1	V_{OH}	0,6	–	0,8	V
open voltage LOW } note 1	V_{OL}	0	–	0,4	V
input voltage LOW	V_{IL}	−0,4	0	0,4	V
input voltage HIGH	V_{IH}	2,0	–	5,0	V
Outputs Q_{1A}, Q_{2A}, Q_{3A}, Q_{4F}, Q_{5F}, Q_{6A}, Q_{7A}, Q_{8F}, Q_{9A}, Q_{13}					
output voltage HIGH	V_{QH}	–	–	12	V
output voltage LOW; I_{QL} = 40 mA	V_{QL}	–	–	0,5	V
output current LOW; note 2	I_{QL}	–	–	60	mA
Outputs Q_{10}, Q_{11}, Q_{12}, Q_{14}, Q_{15}					
output voltage HIGH	V_{OH}	–	–	12	V
output voltage LOW; I_{QL} = 80 mA	V_{QL}	–	–	0,5	V
output current LOW; note 2	I_{QL}	–	–	120	mA
Oscillator connections OSC, QRZ					
frequency	f	–	4,0	–	MHz
input voltage HIGH; QRZ	V_{IH}	2,6	–	5,0	V
input voltage LOW; QRZ	V_{IL}	−2,0	–	2,0	V
input resistance QRZ	R_I	50	–	–	kΩ
input capacitance QRZ	C_I	–	–	5,0	pF
open voltage QRZ	V_{IO}	–	2,25	–	V
open voltage OSC	V_{IO}	–	1,5	–	V
Output GATE					
output voltage LOW; I_{QL} = 20 mA	V_{QL}	–	–	1,0	V
output voltage HIGH; I_{QH} = 0	V_{QH}	–	–	12	V
Output Q_{IF}					
output voltage; conductive	V_Q	2,2	2,5	2,8	V
output voltage; non-conductive	V_Q	–	–	12	V
output resistance; conductive	R_Q	350	500	650	Ω
output resistance; non-conductive	R_Q	50	–	–	kΩ

Notes

1. When this pin is left open it acts as an output at which the number of serial offset pulses for the i.f. offset can be obtained.
2. Peak current for sinusoidal voltage.

APPLICATION INFORMATION

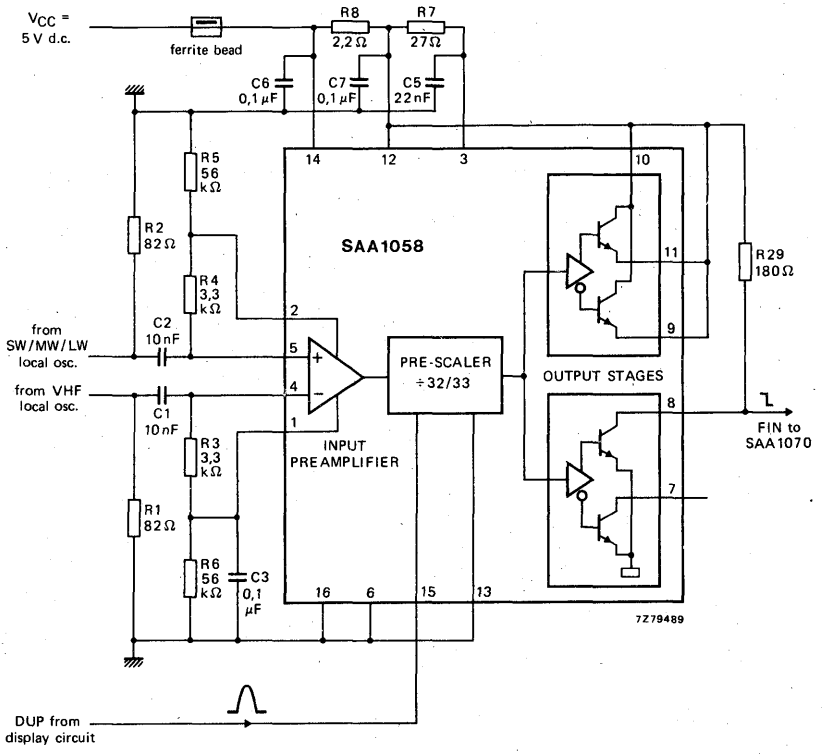


Fig. 3 Pre-scaler circuit for the frequency measurement system; to be used in combination with Fig. 4.

APPLICATION INFORMATION (continued)

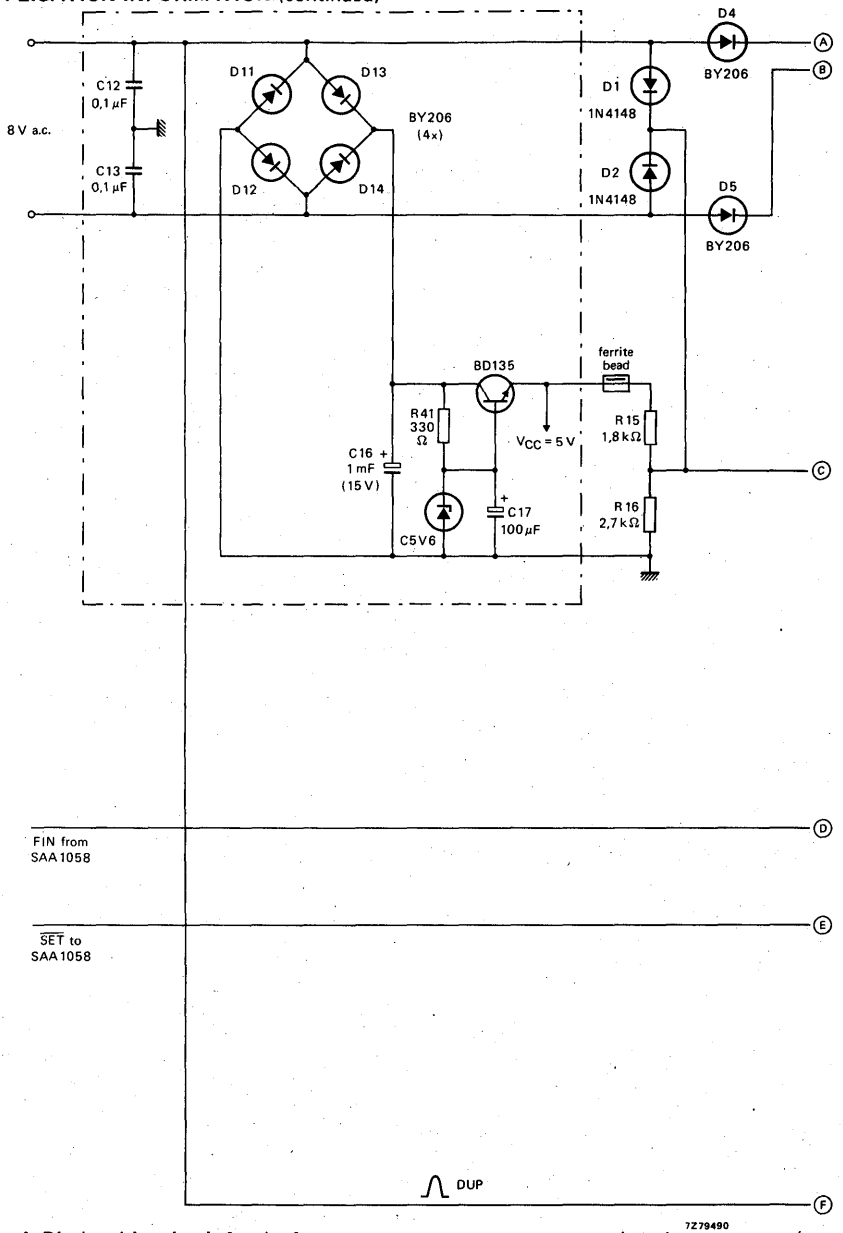
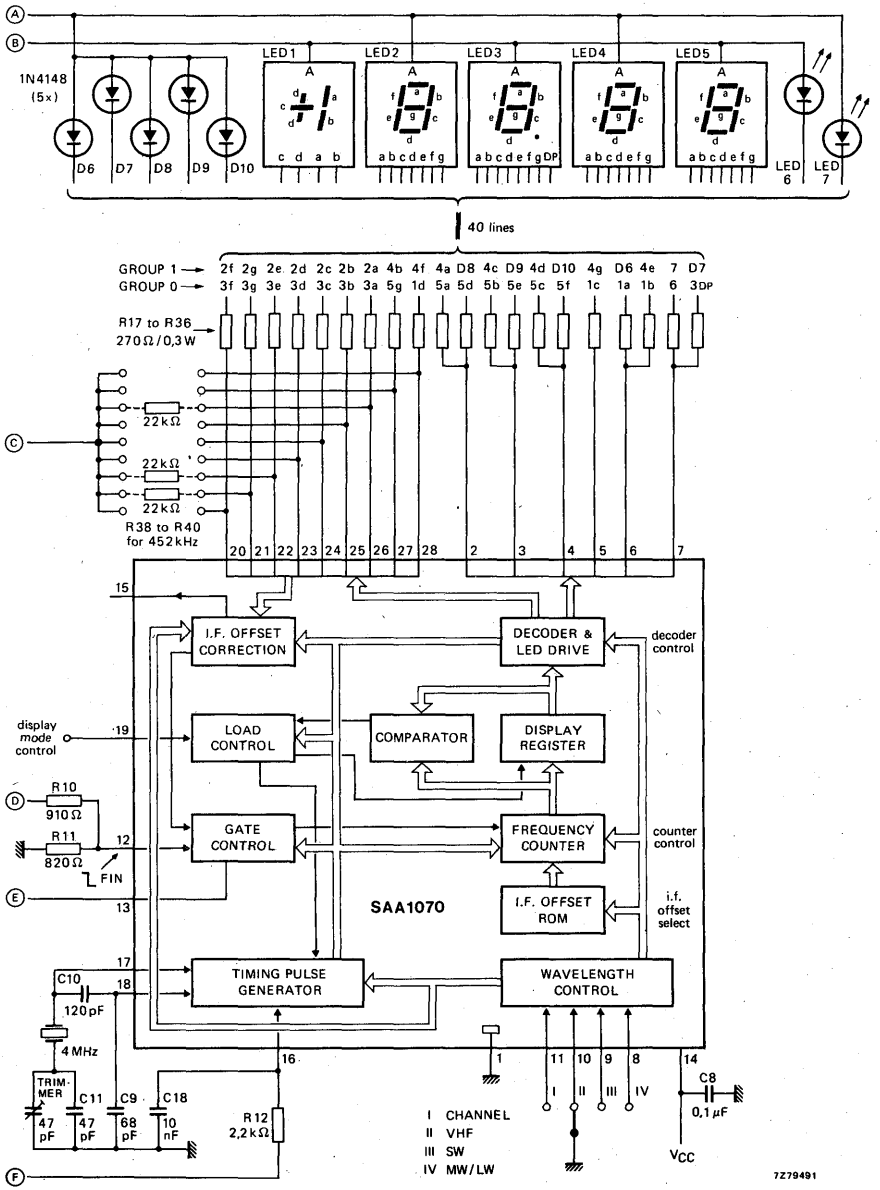


Fig. 4 Display drive circuit for the frequency measurement system; continued on next page (see also Fig. 3).


A
B
1N4148
(5x)
D6
D7
D8
D9
D10
LED1
LED2
LED3
LED4
LED5
LED 6
LED 7
c d a b
a b c d e f g
a b c d e f g DP
40 lines
GROUP 1
GROUP 0
2f 2g 2e 2d 2c 2b 2a 4b 4f 4a D8 4c D9 4d D10 4g D6 4e 7 D7
3f 3g 3e 3d 3c 3b 3a 5g 1d 5a 5d 5b 5e 5c 5f 1c 1a 1b 6 3DP
R17 to R36
270Ω/0,3W
22kΩ
22kΩ
22kΩ
R38 to R40
for 452kHz
C
20 21 22 23 24 25 26 27 28 2 3 4 5 6 7
15
I.F. OFFSET CORRECTION
DECODER & LED DRIVE
decoder control
display mode control
19
LOAD CONTROL
COMPARATOR
DISPLAY REGISTER
D
R10
910Ω
R11
820Ω
FIN
12
GATE CONTROL
FREQUENCY COUNTER
counter control
E
13
SAA1070
I.F. OFFSET ROM
i.f. offset select
17
C10
120pF
18
TIMING PULSE GENERATOR
WAVELENGTH CONTROL
4MHz
16
1
11 10 9 8
14
TRIM-MER
C11
C9
C18
47 pF
47 pF
68 pF
10 nF
R12
2,2kΩ
I CHANNEL
II VHF
III SW
IV MW/LW
I II III IV
C8
0,1μF
VCC
F
7Z79491