125 MHz AMPLIFIER AND DIVIDER-BY-32/33

The silicon monolithic integrated circuit SAA1058 is designed as a programmable-ratio divide-by-32/33 prescaler. It is intended for use in digital radio tuning systems and frequency counters in radio applications with an input frequency range from 0,5 to 125 MHz. The high-frequency inputs are differential inputs of a preamplifier for handling a.m. as well as f.m. oscillator signals. One output set provides complementary ECL levels by emitter followers and a second output buffer set is intended to drive MOS circuits by open collectors.

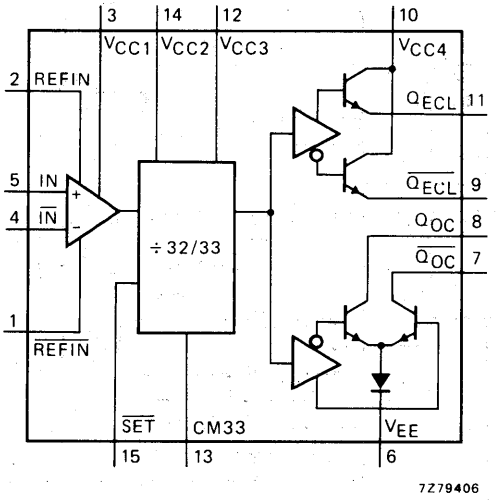


Fig. 1 Block diagram.

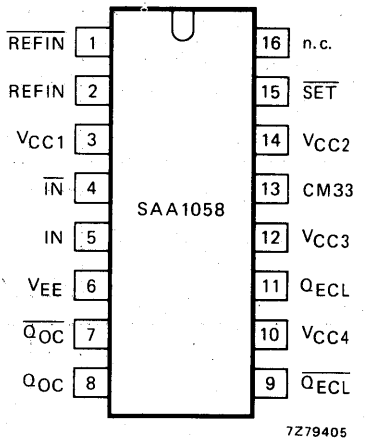


Fig. 2 Pin diagram.
$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = 5$ V
$V_{EE} = 0$ V (ground)
Pin 16 preferably connected to V_{EE}

QUICK REFERENCE DATA

Supply voltage	V_{CC}		5 ± 10% V
Input frequency range	f_i		0,5 to 125 MHz
Input voltage range			
f = 0,5 to 30 MHz	$V_{i(rms)}$		5 to 100 mV
f = 30 to 125 MHz	$V_{i(rms)}$		10 to 100 mV
Power consumption per package (no load)	P_{av}	typ.	550 mW

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

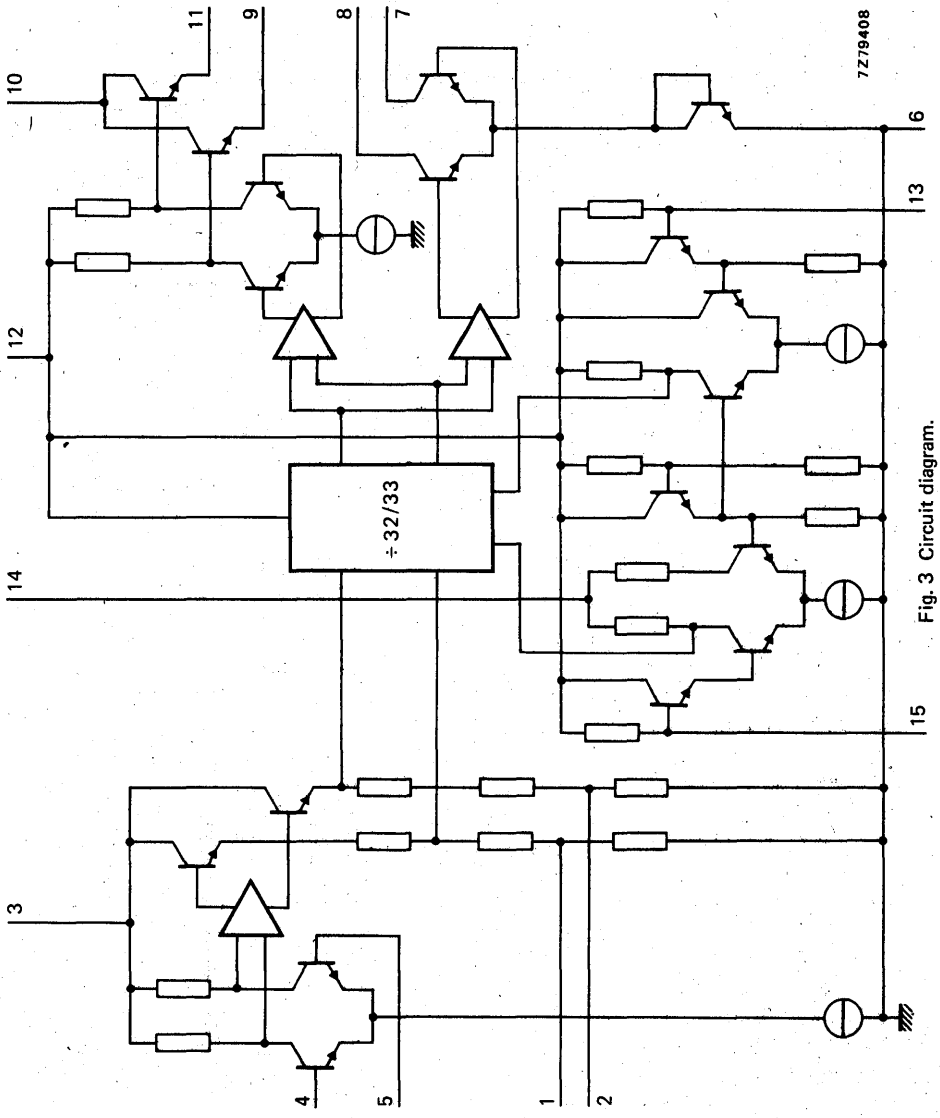


Fig. 3 Circuit diagram.

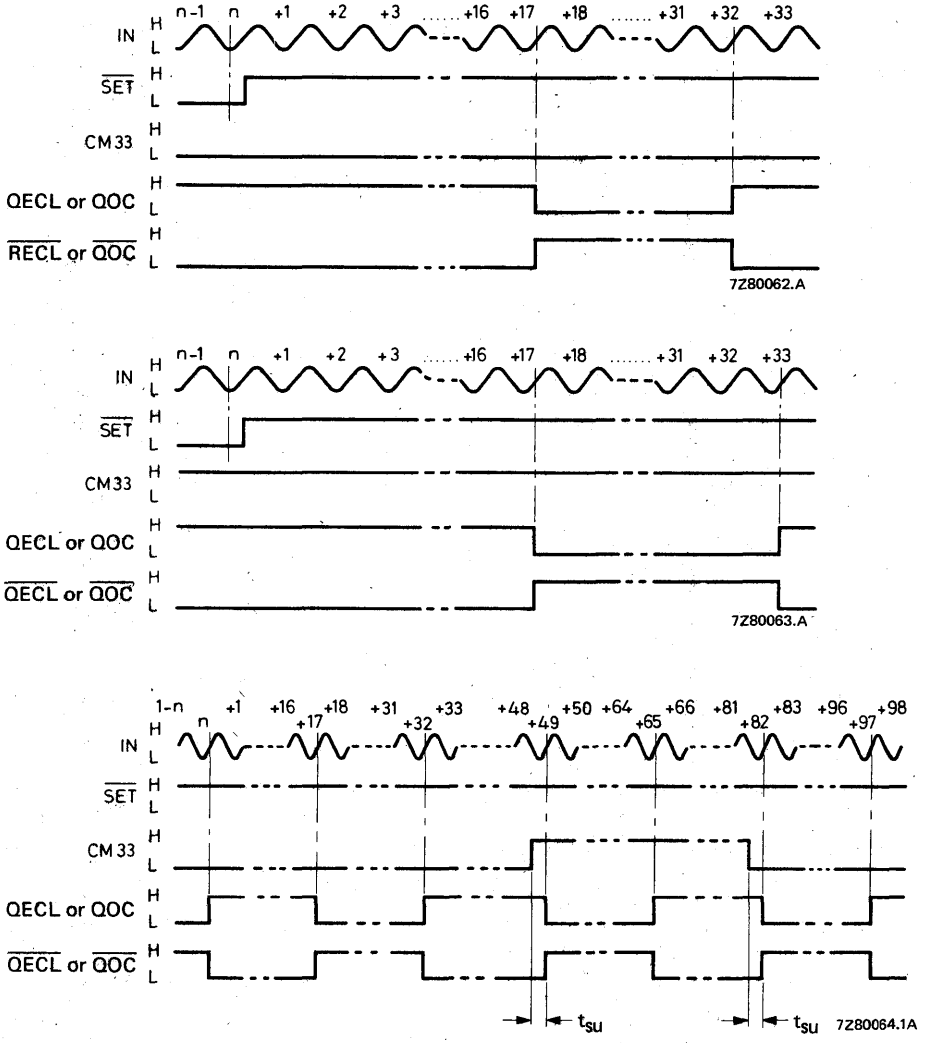


Fig. 4 Timing diagrams of programmable frequency dividing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 3, 10, 12 and 14)	V_{CC}	max.	7 V
Output supply voltage (pins 7 and 8, R_L = 470 Ω)	V_{DD}	max.	14 V
Input voltage	V_I	0 to V_{CC}	
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	0,76 W
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 60	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V (see Fig. 6); T_{amb} = 25 °C, unless otherwise specified.

Supply current ($I_3 + I_{10} + I_{12} + I_{14}$)*	I_{CC}	typ. <	110 mA 135 mA
Count input voltage (pins 4 and 5)			
A.M. (0,5 MHz to 30 MHz)	$V_{i(rms)}$	5 to 100	mV
F.M. (30 MHz to 125 MHz)	$V_{i(rms)}$	10 to 100	mV
A.C. input impedance	R_i	>	1 kΩ
Count mode input (pin 13)			
input voltage for division-ratio 32	V_{CML}	<	2 V
input voltage for division-ratio 33	V_{CMH}	>	3 V
input current at V_{CM} = 2 V	$-I_{CML}$	<	3,5 mA
Set-up time changing the division-ratio from 32 to 33 or vice versa	t_{su}	typ.	50 ns
Input capacitance	C_{CM}	typ.	1 pF
Reset input voltage (pin 15)			
reset	V_{RL}	<	2 V
no reset	V_{RH}	>	3 V
Input current at V_R = 2 V	$-I_{RL}$	<	2 mA
Emitter follower outputs (pins 9 and 11)			
output voltage; R_L = 4,7 kΩ to ground	V_{OH} V_{OL}	> <	3,7 V 3,3 V
Open collector outputs (pins 7 and 8)			
V_{DD} = 11 V; R_L = 470 Ω			
Output voltage HIGH	V_{OH}	>	9 V
Output voltage LOW	V_{OL}	<	2 V

* See Fig. 6.

CHARACTERISTICS (continued)

Open collector outputs (pins 7 and 8) transition times, no capacitive load	t_{TLH}	typ.	15 ns
	t_{THL}	typ.	12 ns

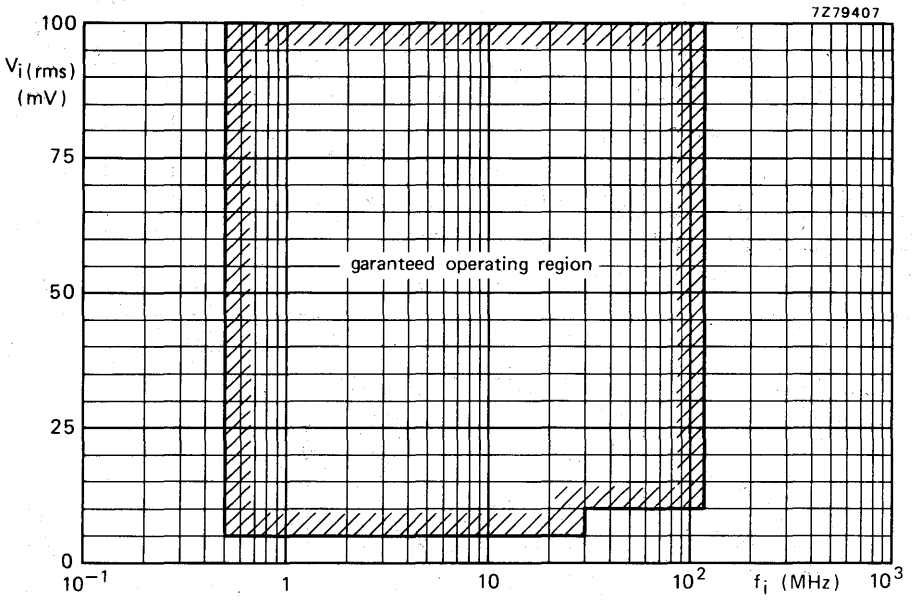


Fig. 5 Triggering level requirements.

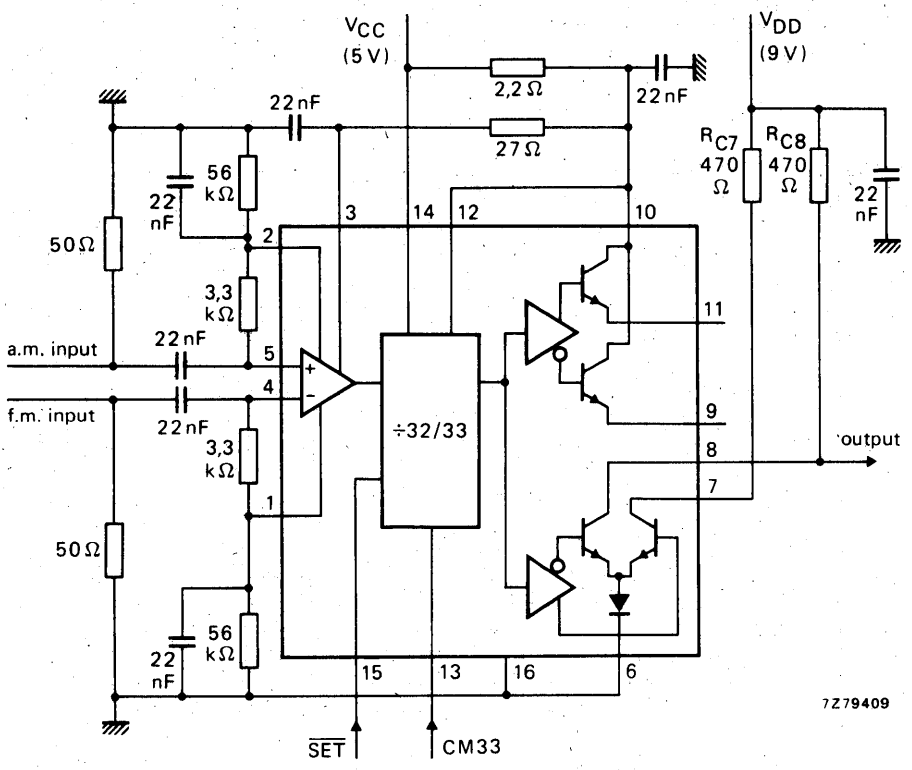
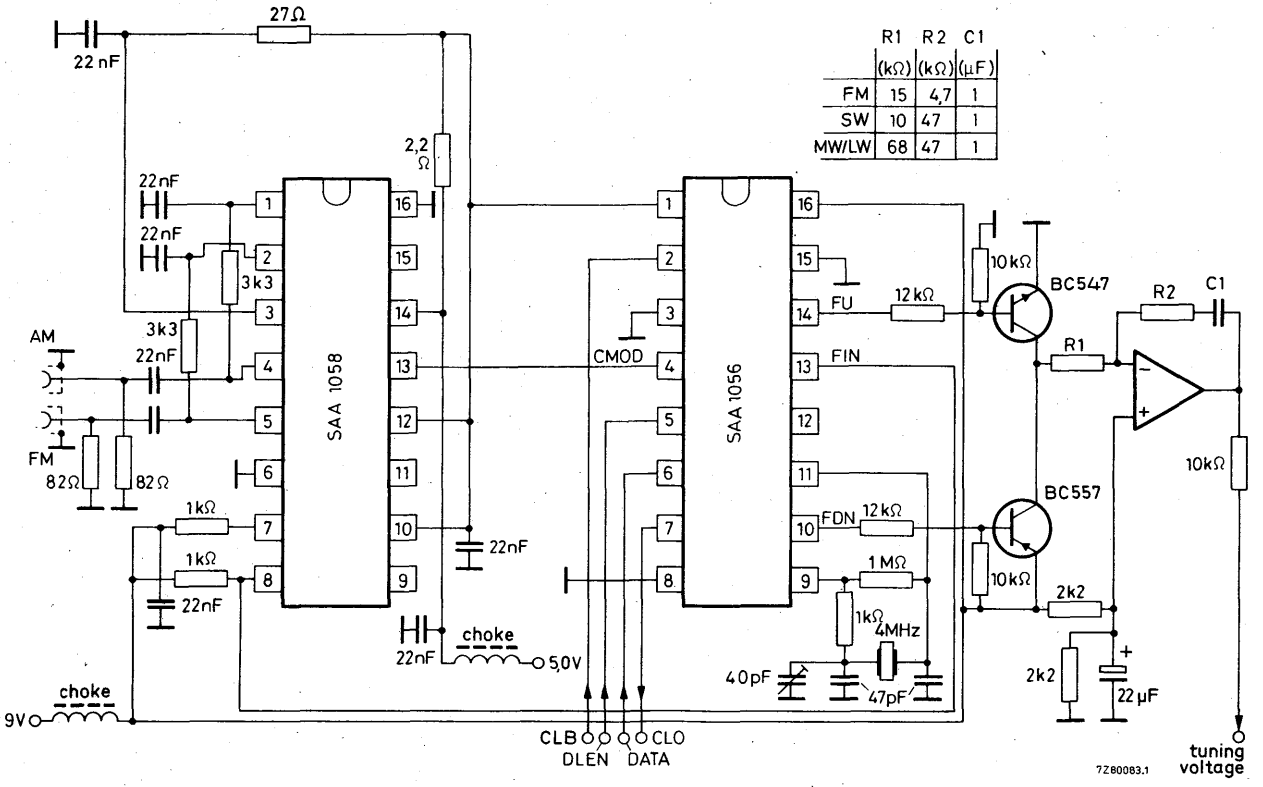


Fig. 6 Test circuit.

APPLICATION INFORMATION



	R1 (kΩ)	R2 (kΩ)	C1 (µF)
FM	15	4,7	1
SW	10	47	1
MW/LW	68	47	1

Fig. 7 Typical application of the SAA1056 with the SAA1058 in a radio receiver.

APPLICATION INFORMATION

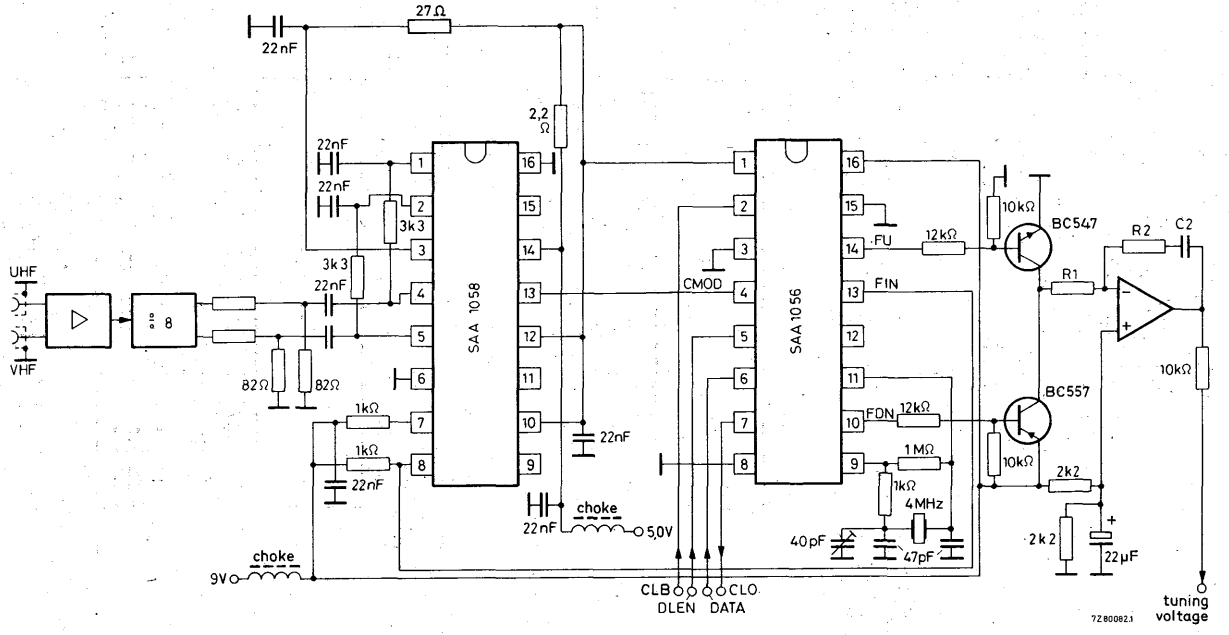


Fig. 8 Typical application of the SAA1056 with the SAA1058 in a TV receiver.