

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PCF21XX FAMILY

SUPERSEDES DATA OF DECEMBER 1987

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
● LCD segments	40	60	64	32
● LED segments	—	2	—	—
● Multiplex rate	1:2	1:2	1:2	1:1
● Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:

PCF2111P: 40-lead DIL; plastic (SOT129).

PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:

PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).

PCF2112T:



PHILIPS

October 1990

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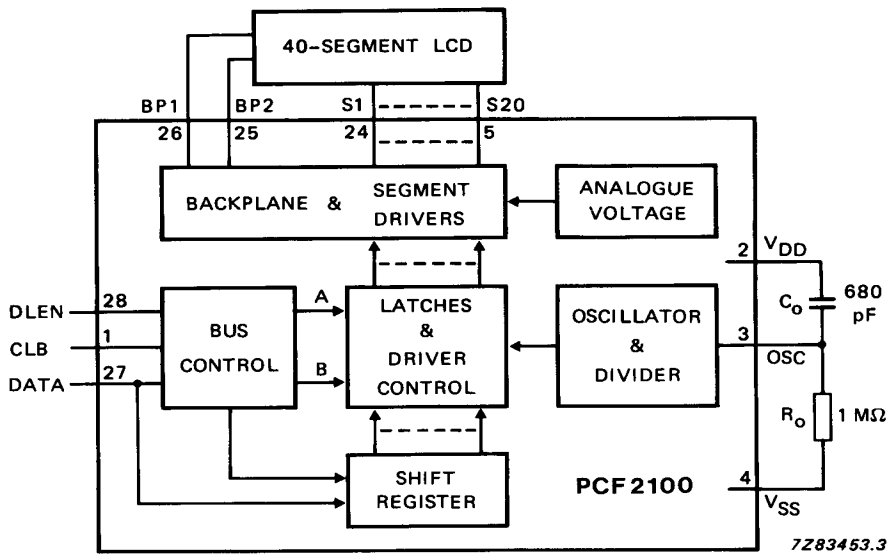


Fig. 1 Block diagram; PCF2100

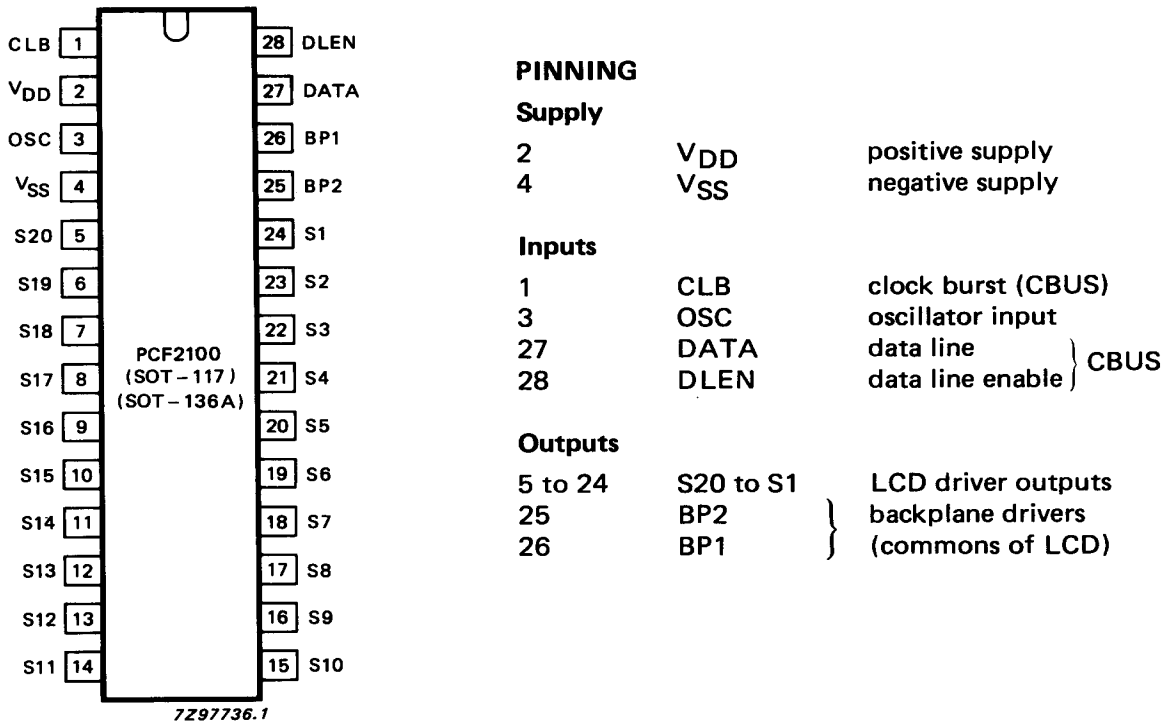


Fig. 2 Pinning diagram; PCF2100

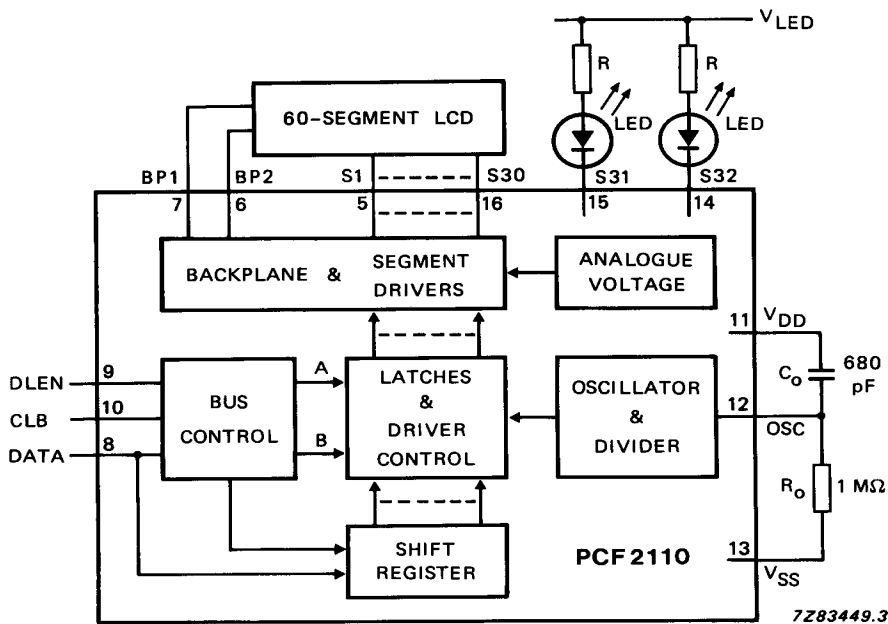


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

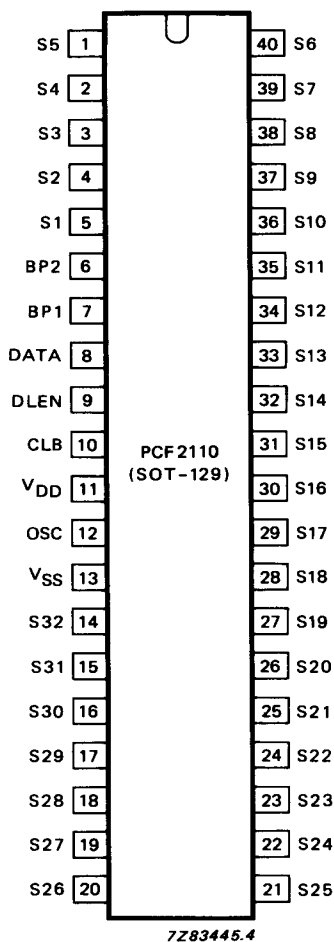


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	VDD	positive supply
13	VSS	negative supply

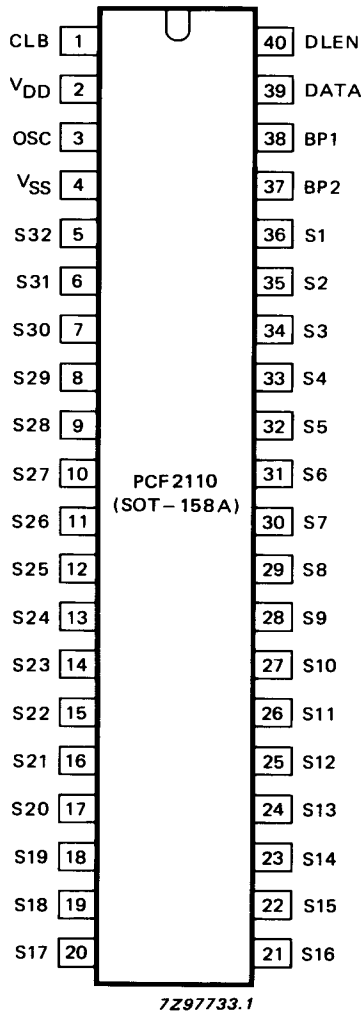
Inputs

8	DATA	data line } CBUS	
9	DLEN		data line enable
10	CLB		clock burst
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	
7	BP1	(commons of LCD)
14	S32	LED driver outputs
15	S31	
16 to 40	S30 to S6	LCD driver outputs





PINNING (SOT-158A)

Supply

2	V _{DD}	positive supply
4	V _{SS}	negative supply

Inputs

1	CLB	} CBUS
3	OSC	
39	DATA	
40	DLEN	data line enable

Outputs

5	S32	} LED driver outputs
6	S31	
7 to 36	S30 to S1	} LCD driver outputs
37	BP2	
38	BP1	} backplane drivers (commons of LCD)

Fig. 5 Pinning diagram; PCF2110



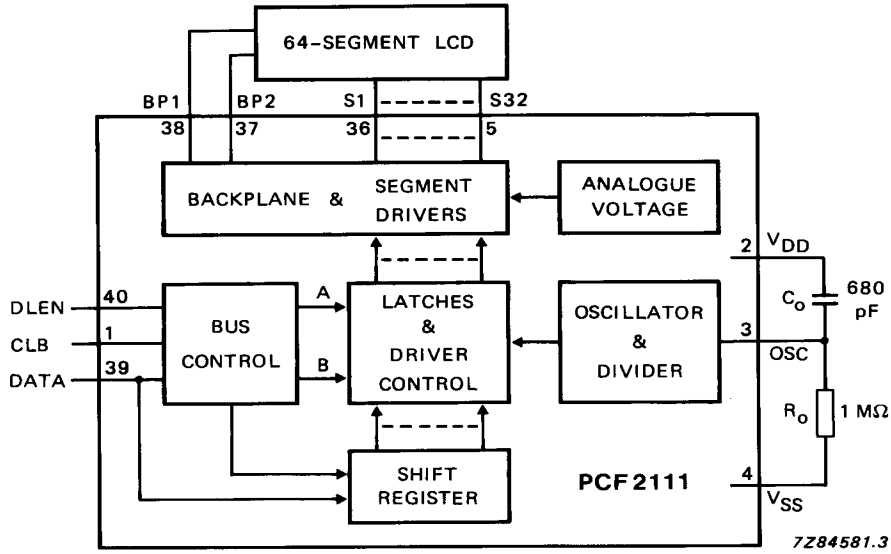
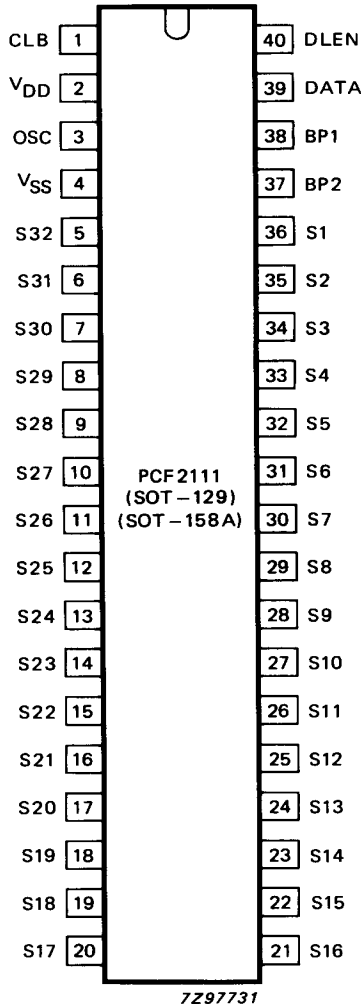


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA



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Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2 VDD positive supply
4 VSS negative supply

Inputs

1 CLB clock burst (CBUS)
3 OSC oscillator input
39 DATA data line
40 DLEN data line enable } CBUS

Outputs

5 to 36 S32 to S1 LCD driver outputs
38 BP1 backplane drivers
37 BP2 (commons of LCD)



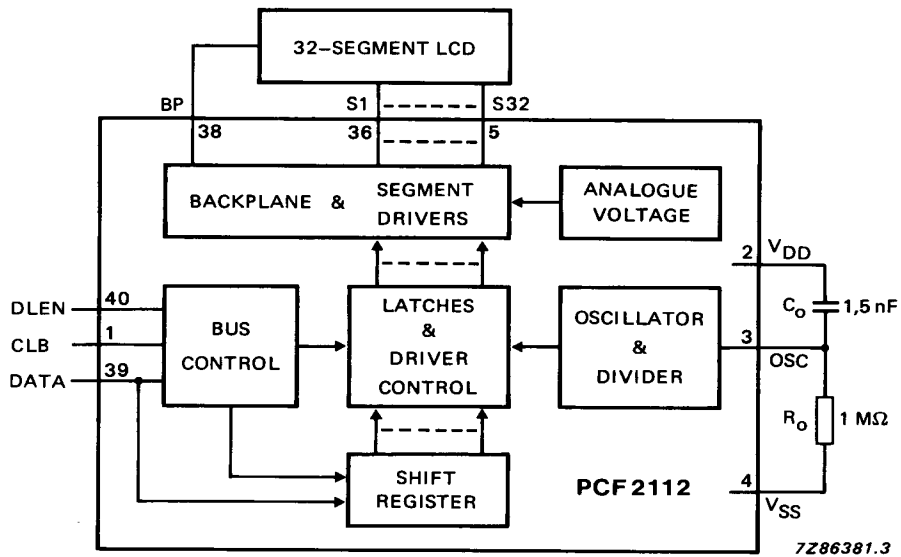


Fig. 8 Block diagram; PCF2112

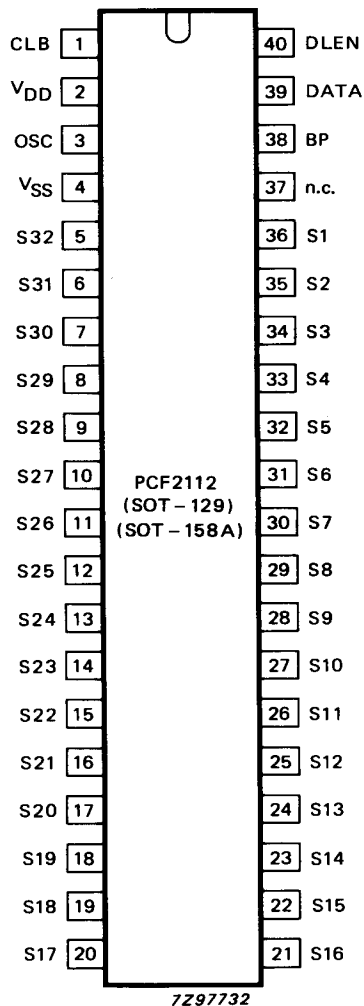


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V _{DD}	positive supply
4	V _{SS}	negative supply

Inputs

1	CLB	} CBUS
3	OSC	
39	DATA	
40	DLEN	data line enable

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

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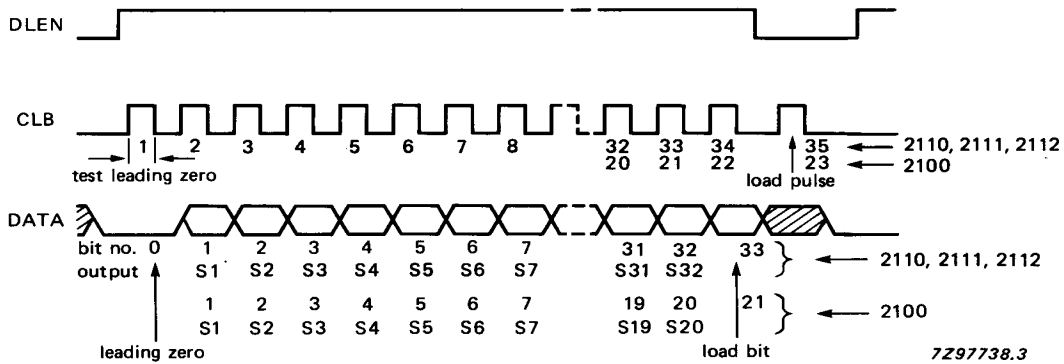


Fig. 10 CBUS data format.

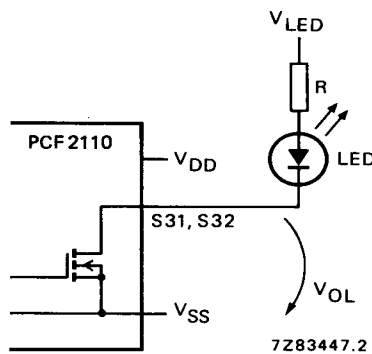


Fig. 11 LED driver circuitry.



The following tests are carried out by the bus control logic:

- a. Test on leading zero.
- b. Test on number of DATA-bits.
- c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

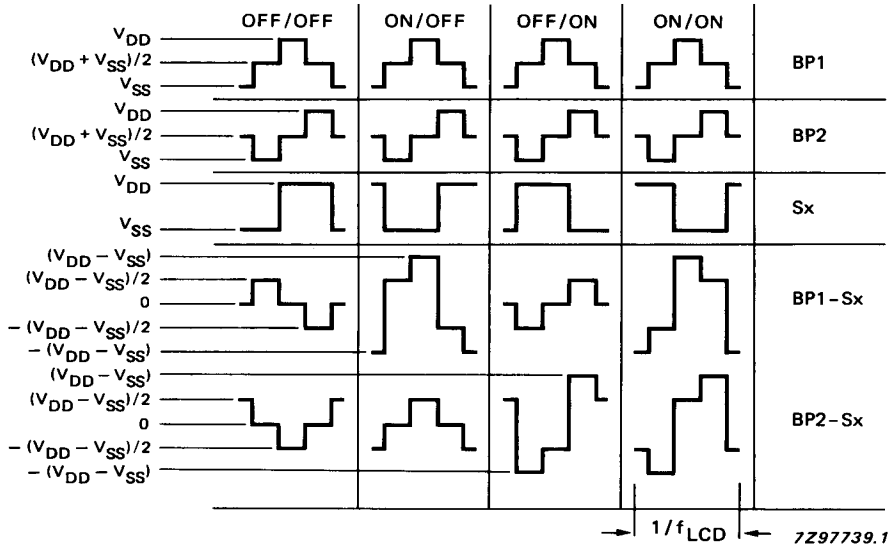


Fig. 12 Timing diagram (except PCF2112).

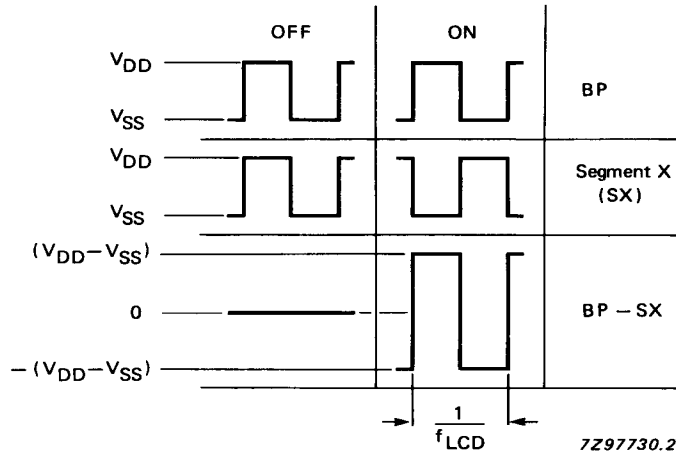


Fig. 13 Timing diagram for PCF2112.

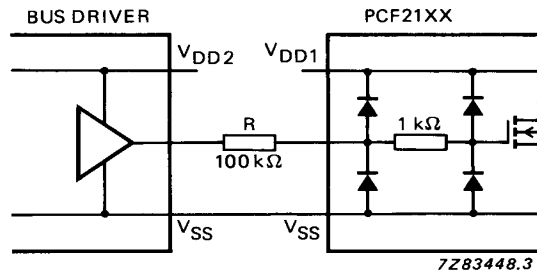


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0,5 V$, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leq 40 \mu A$.

DEVELOPMENT DATA

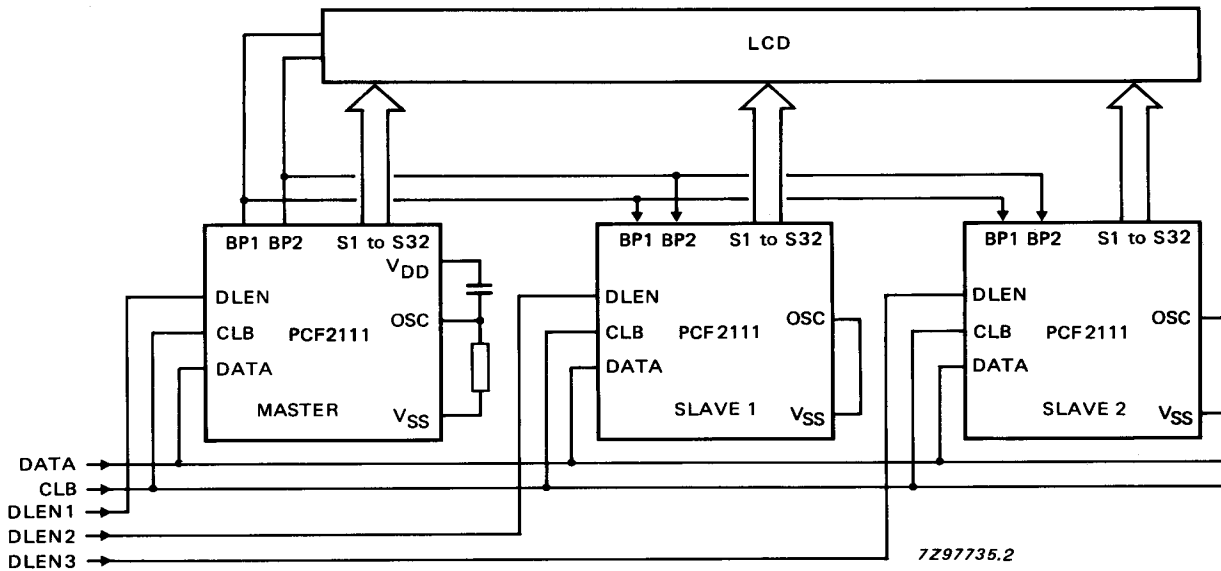


Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	-0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	$V_{SS}-0,5$	$V_{DD}+0,5$	V
Output voltage range BP1, BP2 and S1 to S32		V_O	$V_{SS}-0,5$	$V_{DD}+0,5$	V
Supply current		$\pm I_{DD}, \pm I_{SS}$	-	50	mA
DC input current		$\pm I_I$	-	20	mA
DC output current		$\pm I_O$	-	25	mA
Total power dissipation per package	note 1	P_{tot}	-	500	mW
Power dissipation per output		P_O	-	100	mW
Storage temperature range		T_{stg}	-65	+ 150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').



DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_{DD} = 2,25\text{ to }6,5\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$; $R_O = 1\text{ M}\Omega$; $C_O = 680\text{ pF}$; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	—	6,5	V
Supply current	note 1	I_{DD1}	—	20	50	μA
Supply current	note 1; $T_{amb} = 25\text{ }^{\circ}\text{C}$	I_{DD2}	—	20	30	μA
Power-on reset level	note 2	V_{POR}	—	1,0	1,6	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	—	—	0,8	V
HIGH		V_{IH}	2,0	—	—	V
Leakage current	$V_I = V_{SS}\text{ or }V_{DD}$	$\pm I_I$	—	—	1	μA
Input capacitance	note 3	C_I	—	—	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	—	20	—	mV
Backplane driver output impedance	note 4; $V_{DD} = 5\text{ V}$	R_{BP}	—	0,5	5	$\text{k}\Omega$
Segment driver output impedance	note 4; $V_{DD} = 5\text{ V}$	R_S	—	1	7	$\text{k}\Omega$
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	$V_{OL} = 0,4\text{ V}; V_{DD} = 5\text{ V}$	I_{OL}	8	14	—	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	—	—	1	μA
Load current		I_{LED}	—	—	20	mA

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AC CHARACTERISTICS (note 5)

$V_{SS} = 0\text{ V}$; $V_{DD} = 2,25\text{ to }6,5\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$; $R_O = 1\text{ M}\Omega$; $C_O = 680\text{ pF}$; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	—	—	μs
Data hold time		t_{HDDA}	3	—	—	μs
Enable set-up time		t_{SUEN}	1	—	—	μs
Disable set-up time		t_{SUDI}	2	—	—	μs
Load pulse set-up time		t_{SULD}	2,5	—	—	μs
Busy time		t_{BUSY}	3	—	—	μs
CLB HIGH time		t_{WH}	1	—	—	μs
CLB LOW time		t_{WL}	5	—	—	μs
CLB period		t_{CLB}	10	—	—	μs
Rise and fall times		t_r, t_f	—	—	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	$C_O = 1,5\text{ nF}$	f_{LCD}	30	35	50	Hz
Transfer time with test loads	$V_{DD} = 5\text{ V}$	t_{BS}	—	20	100	μs
Driver delay with test loads	$V_{DD} = 5\text{ V}$	t_{PLCD}	—	20	100	μs



Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD} .

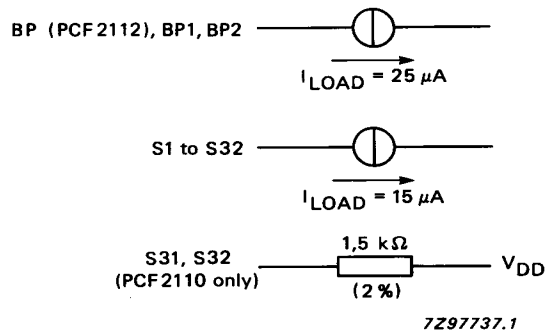
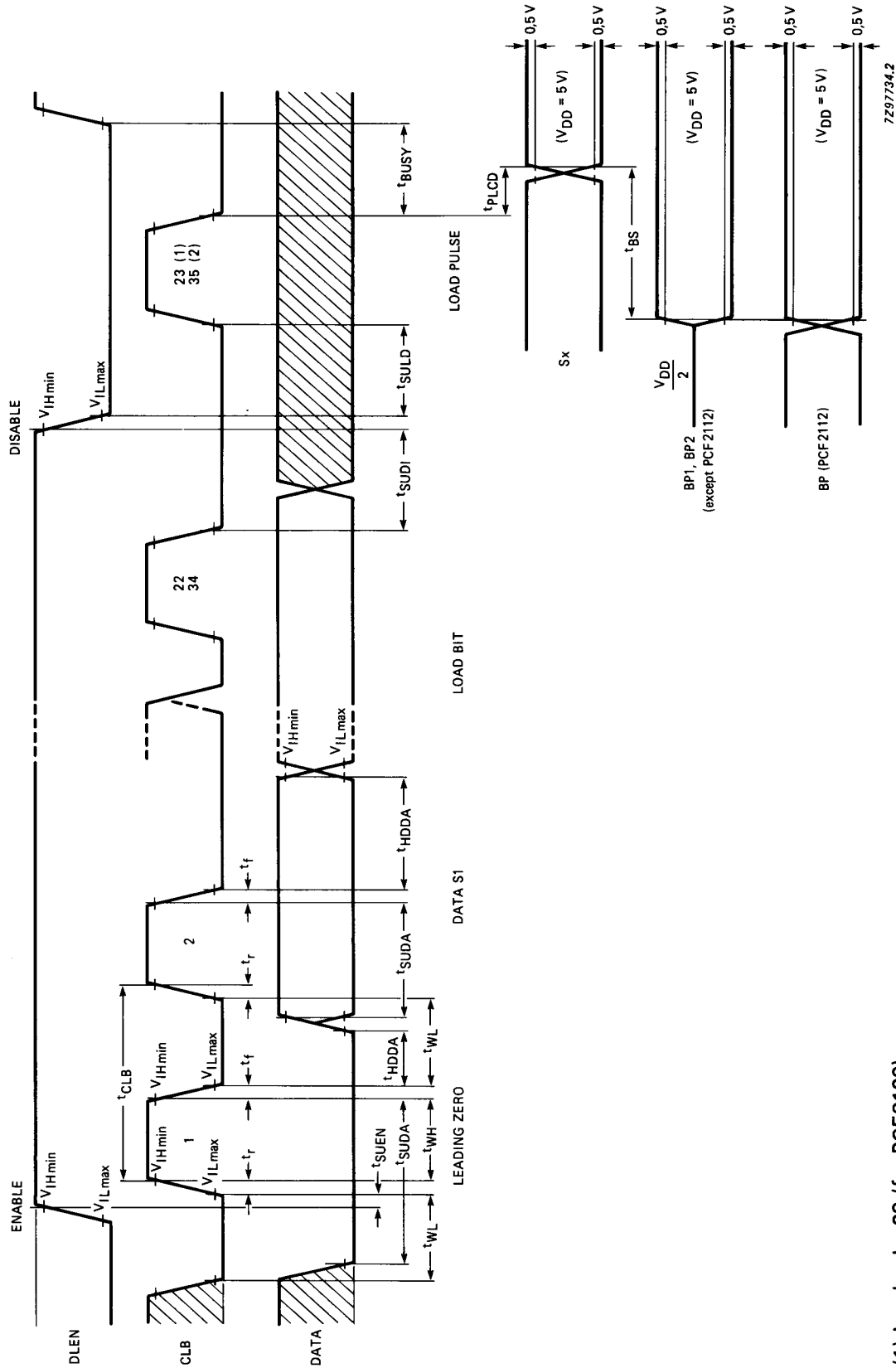


Fig. 16 Test loads.

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(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

Fig. 17 CBUS timing.

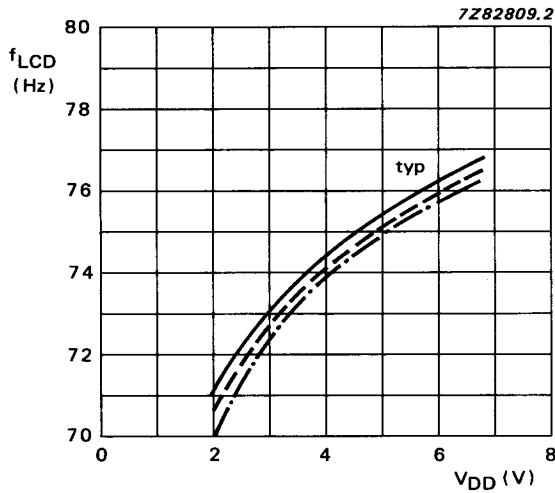


Fig. 18 Displays frequency as a function of supply voltage; $C_O = 680 \text{ pF}$ (except PCF2112).

— $T_{amb} = -40 \text{ }^\circ\text{C}$;
 - - - $T_{amb} = +25 \text{ }^\circ\text{C}$;
 - . . - $T_{amb} = +85 \text{ }^\circ\text{C}$.

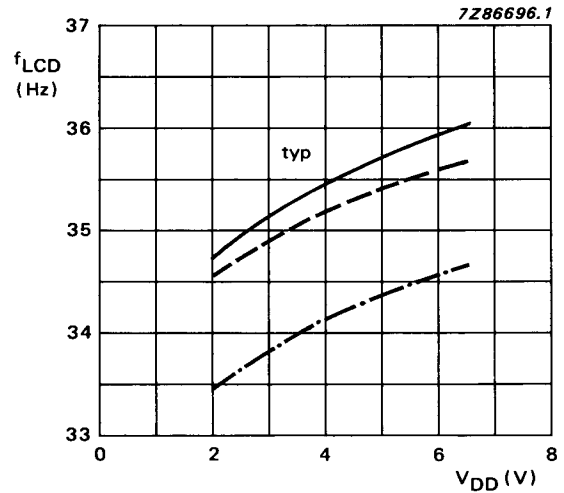


Fig. 19 Display frequency as a function of supply voltage; $C_O = 1,5 \text{ nF}$ (only PCF2112).

— $T_{amb} = -40 \text{ }^\circ\text{C}$;
 - - - $T_{amb} = +25 \text{ }^\circ\text{C}$;
 - . . - $T_{amb} = +85 \text{ }^\circ\text{C}$.

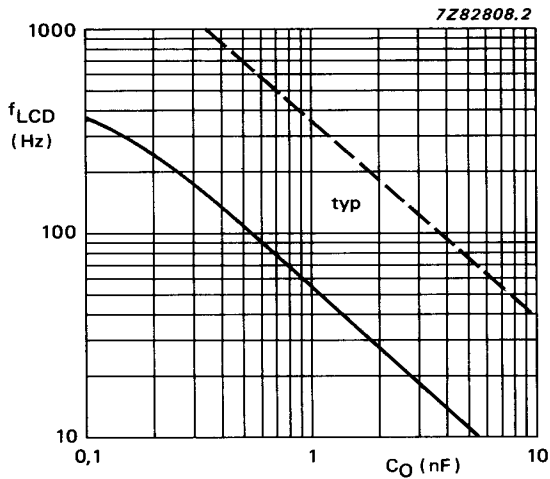


Fig. 20 Display frequency as a function of R_O and C_O ; $T_{amb} = +25 \text{ }^\circ\text{C}$; $V_{DD} = 5 \text{ V}$.

— $R_O = 1 \text{ M}\Omega$;
 - - - $R_O = 100 \text{ k}\Omega$.

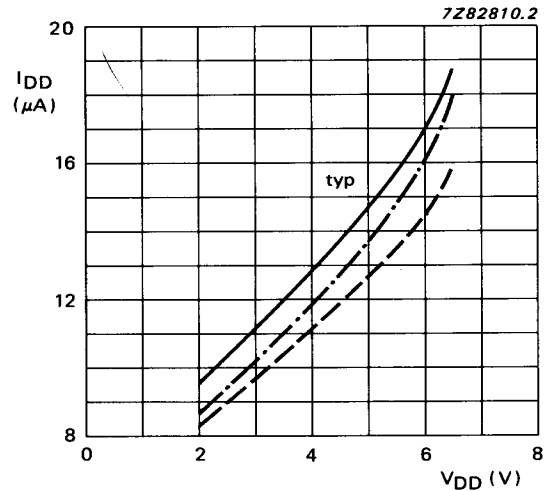


Fig. 21 Supply current as a function of supply voltage.

— $T_{amb} = -40 \text{ }^\circ\text{C}$;
 - - - $T_{amb} = +25 \text{ }^\circ\text{C}$;
 - . . - $T_{amb} = +85 \text{ }^\circ\text{C}$.

DEVELOPMENT DATA



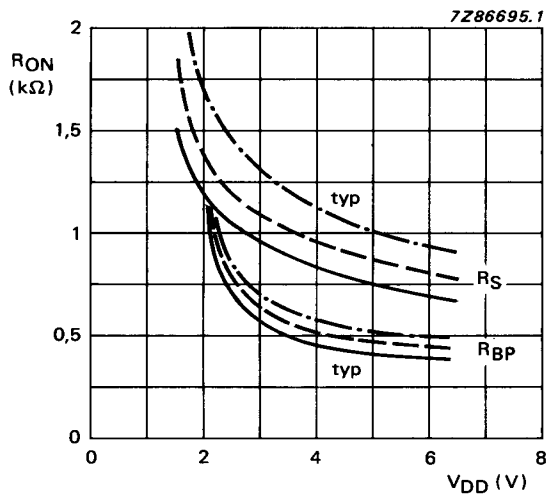


Fig. 22 Output resistance of backplane and segments.

— $T_{amb} = -40\text{ }^{\circ}\text{C}$;
 - - - $T_{amb} = +25\text{ }^{\circ}\text{C}$;
 - . - . $T_{amb} = +85\text{ }^{\circ}\text{C}$.

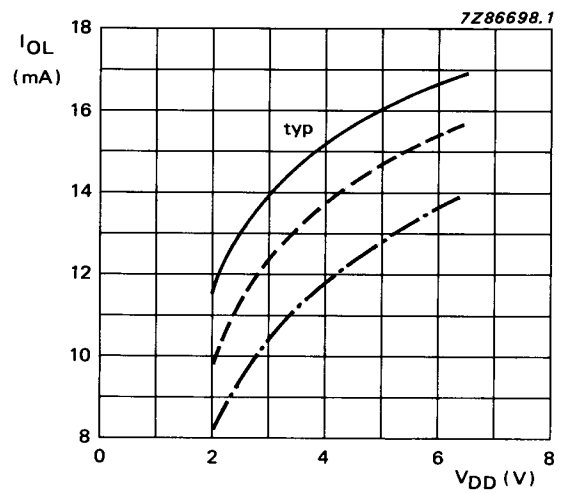
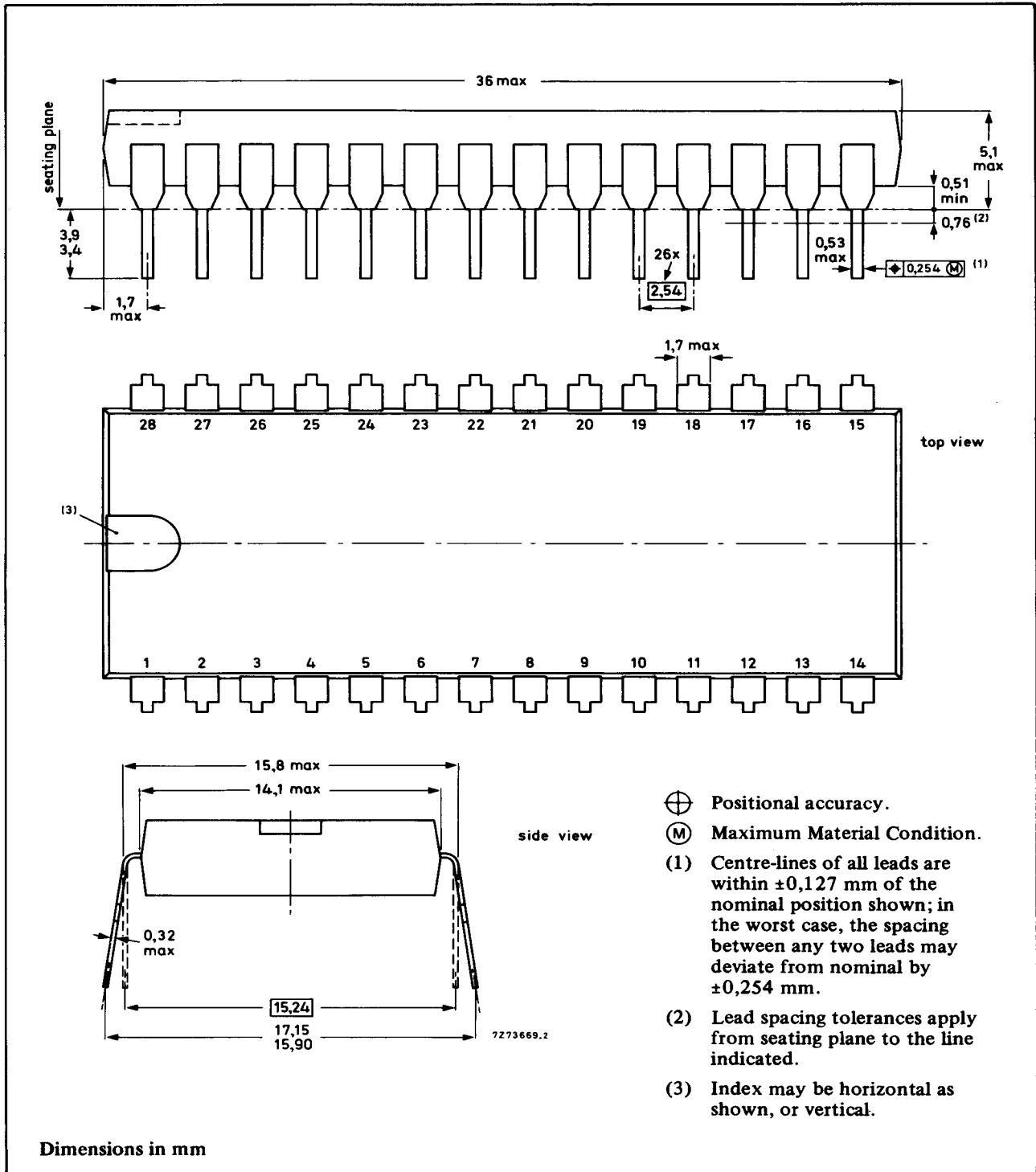


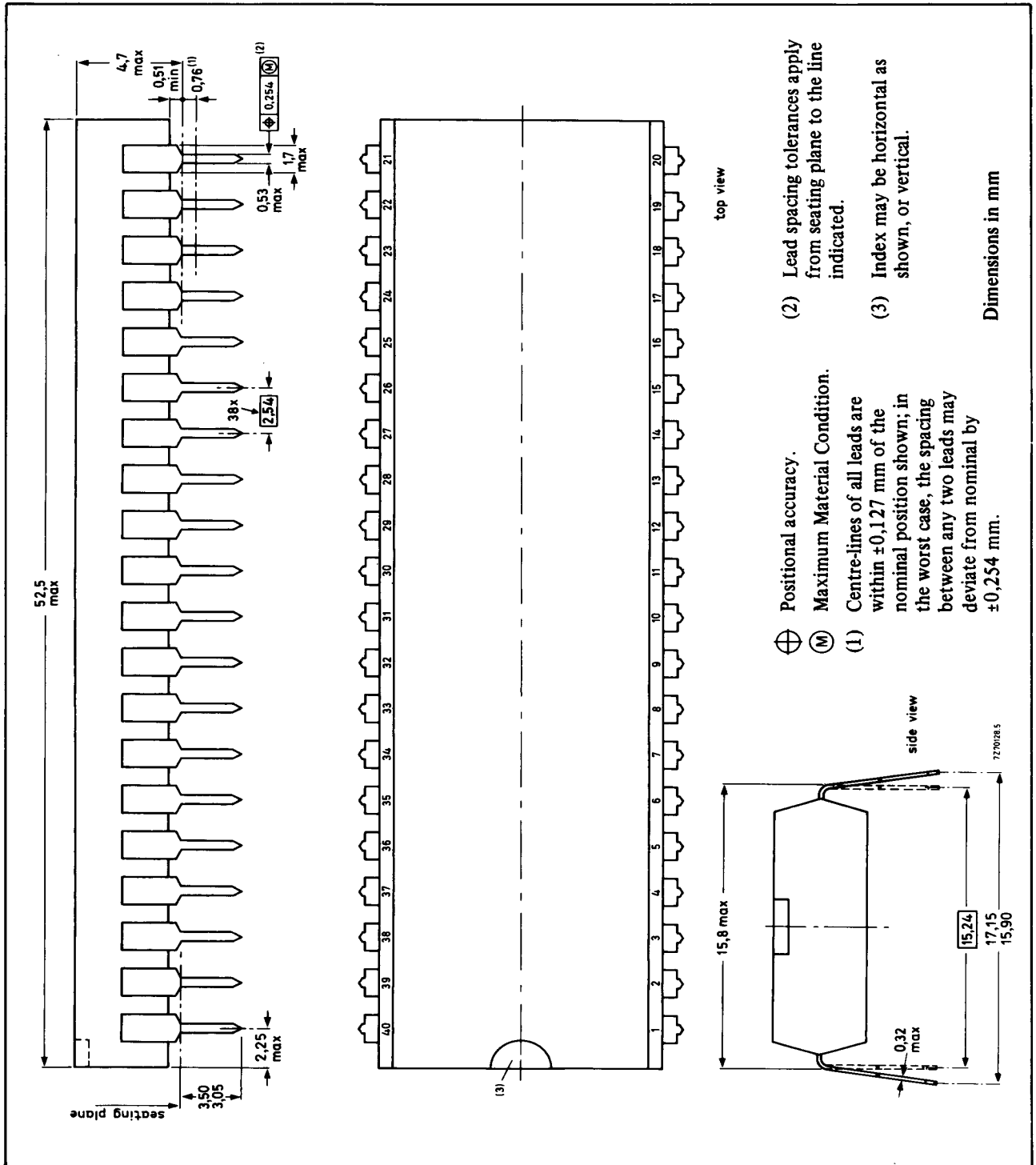
Fig. 23 Output current as a function of supply voltage (only PCF2112).

— $T_{amb} = -40\text{ }^{\circ}\text{C}$;
 - - - $T_{amb} = +25\text{ }^{\circ}\text{C}$;
 - . - . $T_{amb} = +85\text{ }^{\circ}\text{C}$.

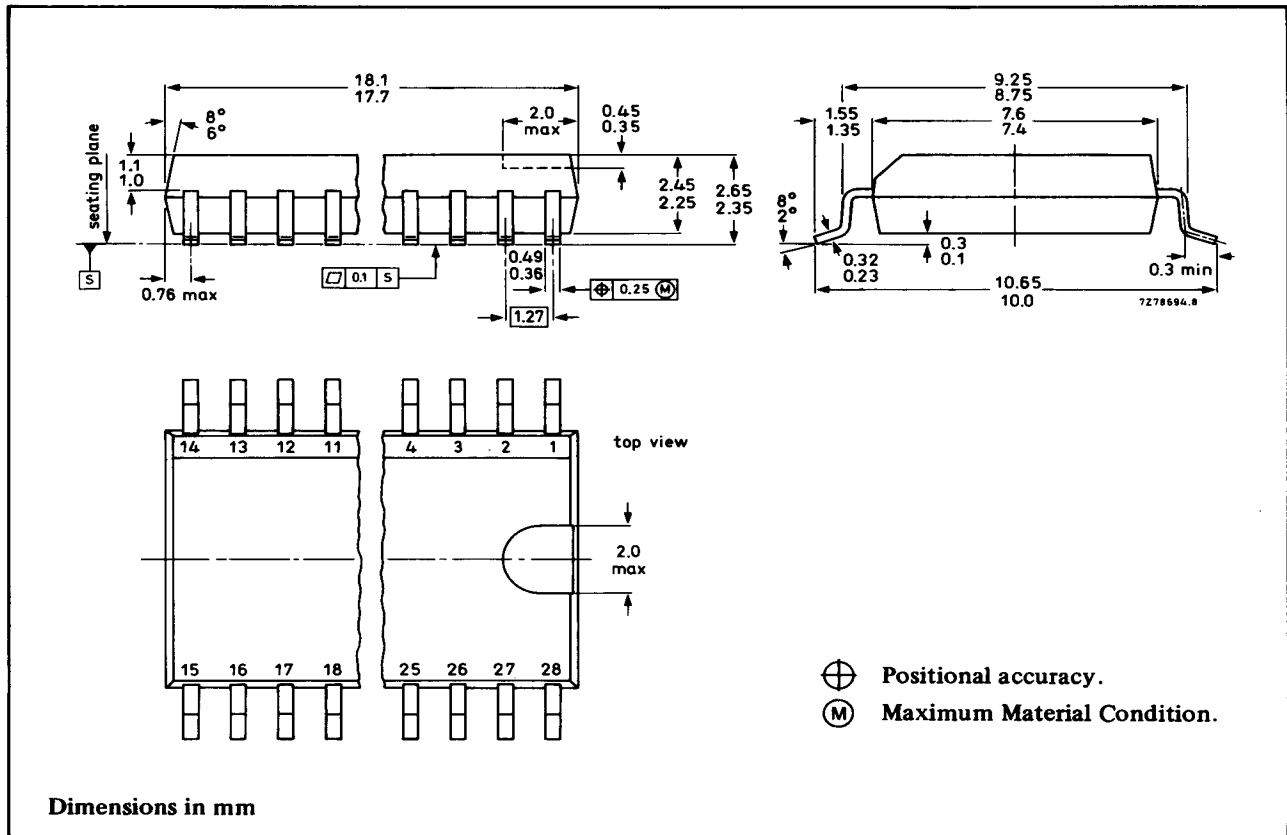
28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



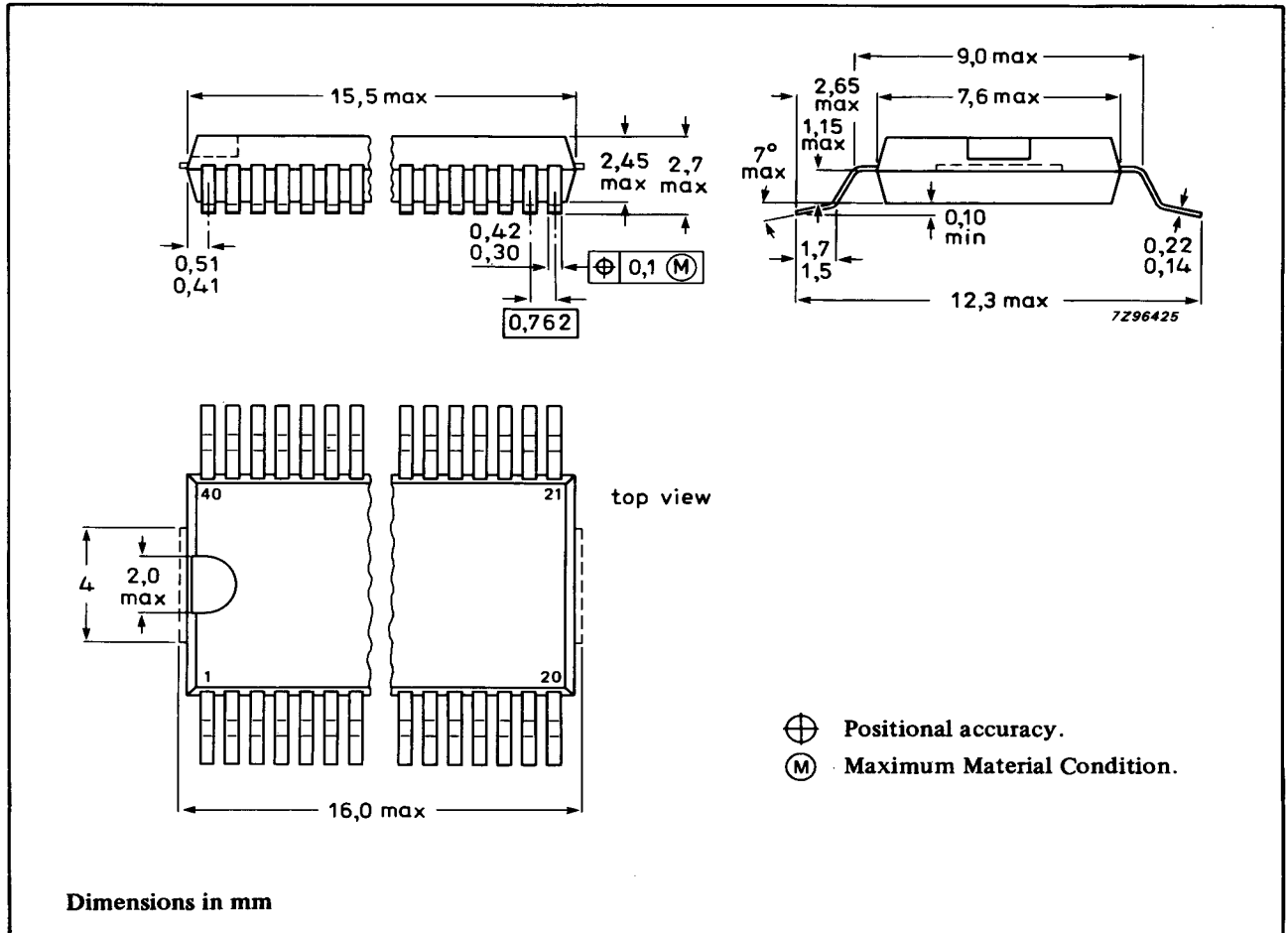
40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



SOLDERING PLASTIC MINI-PACKS**1. By hand-held soldering iron or pulse-heated solder tool**

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement. Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES**1. By hand**

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

