



ISO<sup>2</sup>-CMOS MT8870B/MT8870B-1  
Integrated DTMF Receiver

T-75-27-07

Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Description

The MT8870B/MT8870B-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO<sup>2</sup>-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital

9161-002-051-NA ISSUE 2 December 1987

**Pin Connections**

IN+	1	18	VDD
IN-	2	17	St/GT
GS	3	16	Est
VRef	4	15	Std
IC*	5	14	Q4
IC*	6	13	Q3
OSC1	7	12	Q2
OSC2	8	11	Q1
VSS	9	10	TOE

\* Connect to VSS

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**Ordering Information -40°C to +85°C**

MT8870BE/MT8870BE-1 Plastic DIP  
MT8870BC/MT8870BC-1 CerDip

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counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

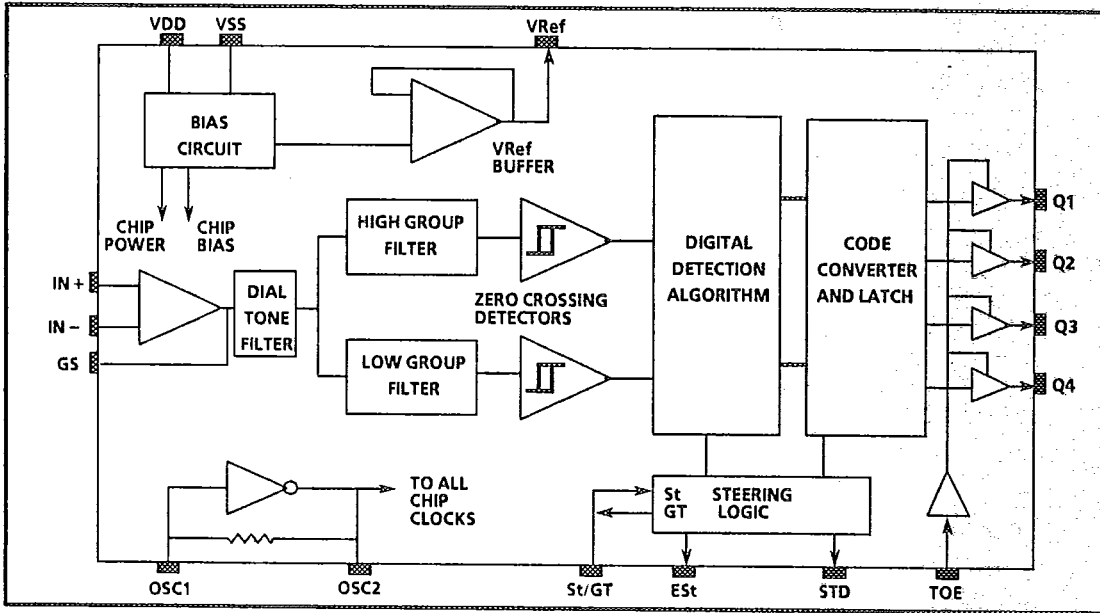


Figure 1 - Functional Block Diagram

# MT8870B/MT8870B-1 ISO<sup>2</sup>-CMOS

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## Absolute Maximum Ratings<sup>1</sup>

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	Parameter	Symbol	Min	Max	Units
1	Power supply voltage $V_{DD}-V_{SS}$			6	V
2	Voltage on any pin		$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current at any pin (other than supply)			10	mA
4	Operating temperature	$T_A$	-40	+85	°C
5	Storage temperature		-65	+150	°C
6	Package power dissipation			1000	mW

<sup>1</sup>Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Derate above 75°C at 16 mW / °C. All leads soldered to board.

## Recommended Operating Conditions - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
1	Positive Supply Voltages	$V_{DD}$		5		V	$V_{SS}=0V$
2	Oscillator Clock Frequency	$f_c$		3.579545		MHz	
3	Oscillator Frequency Tolerance	$\Delta f_c$		$\pm 0.1$		%	

<sup>2</sup>Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## DC Electrical Characteristics- $V_{DD}=5.0V \pm 5\%$ , $V_{SS}=0V$ . Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.

	Characteristics	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
1 S U P P L Y	Operating supply voltage	$V_{DD}$	4.75	5.0	5.25	V	
	Operating supply current	$I_{DD}$		3.0	9.0	mA	
	Power consumption	$P_O$		15	45	mW	$f=3.58\text{ MHz}; V_{DD}=5V$
4 I N P U T S	High level input	$V_{IH}$	3.5			V	
	Low level input voltage	$V_{IL}$			1.5	V	
	Input leakage current	$I_{IH}/I_{IL}$		0.1		$\mu A$	$V_{IN}=V_{SS}\text{ or }V_{DD}$
	Pull-up (source) current	$I_{SO}$		7.5	15	$\mu A$	TOE (pin 10)=0V
	Input impedance ( $IN+$ , $IN-$ )	$R_{IN}$		10		$M\Omega$	@ 1 kHz
9	Steering threshold voltage	$V_{TSt}$	2.2		2.5	V	
10 O U T P U T S	Low level output voltage	$V_{OL}$			$V_{SS}+0.03$	V	No load
	High level output voltage	$V_{OH}$	$V_{DD}-0.03$			V	No load
	Output low (sink) current	$I_{OL}$	1	2.5		mA	$V_{OUT}=0.4V$
	Output high (source) current	$I_{OH}$	0.4	0.8		mA	$V_{OUT}=4.6V$
	$V_{Ref}$ output voltage	$V_{Ref}$	2.4		2.7	V	No load
	$V_{Ref}$ output resistance	$R_{OR}$		10		$k\Omega$	

<sup>2</sup>Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

**Operating Characteristics<sup>1</sup>** - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated.  
**Gain Setting Amplifier** T-75-27-07

	Characteristics	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
1	Input leakage current	$I_{IN}$		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	$R_{IN}$		10		M $\Omega$	
3	Input offset voltage	$V_{OS}$		25		mV	
4	Power supply rejection	PSRR		60		dB	1 kHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \leq V_{IN} \leq 3.0V$
6	DC open loop voltage gain	$A_{VOL}$		65		dB	
7	Open loop unity gain bandwidth	$f_c$		1.5		MHz	
8	Output voltage swing	$V_O$		4.5		$V_{pp}$	$R_L \geq 100K\Omega$ to $V_{SS}$
9	Maximum capacitive load (GS)	$C_L$		100		pF	
10	Maximum resistive load (GS)	$R_L$		50		K $\Omega$	
11	Common mode range	$V_{CM}$		3.0		$V_{pp}$	No Load

<sup>1</sup>  $V_{DD} = 5V, V_{SS} = 0V, T_A = 25^\circ C$

<sup>2</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

**MT8870B AC Electrical Characteristics<sup>1</sup>** - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Notes
1	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
			27.5			mV <sub>RMS</sub>	1,2,3,5,6,9
					+1	dBm	1,2,3,5,6,9
					869	mV <sub>RMS</sub>	1,2,3,5,6,9
2	Positive twist accept			10		dB	2,3,6,9
3	Negative twist accept			10		dB	2,3,6,9
4	Freq. deviation accept		$\pm 1.5\% \pm 2Hz$			Nom.	2,3,5,9
5	Freq. deviation reject		$\pm 3.5\%$			Nom.	2,3,5,9
6	Third tone tolerance			-16		dB	2,3,4,5,9
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

<sup>1</sup>  $V_{DD} = 5V, V_{SS} = 0, T_A = 25^\circ C$  and  $f_c = 3.579545$  MHz using test circuit shown in Figure 2.

**NOTES**

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by  $\pm 1.5\% \pm 2Hz$ .
7. Bandwidth limited (3KHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz)  $\pm 2\%$ .
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. For guard time calculation purposes.

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# MT8870B/MT8870B-1 ISO<sup>2</sup>-CMOS

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## MT8870B-1 AC Electrical Characteristics\* - Voltages are with respect to ground ( $V_{SS}$ ) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Notes	
1	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9	
			21.8			mV <sub>RMS</sub>	1,2,3,5,6,9	
					+1		dBm	1,2,3,5,6,9
					869		mV <sub>RMS</sub>	1,2,3,5,6,9
2	Input Signal Level Reject		-37			dBm	1,2,3,5,6,9	
			10.9			mV <sub>RMS</sub>	1,2,3,5,6,9	
3	Positive twist accept				6	dB	2,3,6,9	
4	Negative twist accept				6	dB	2,3,6,9	
5	Freq. deviation accept		$\pm 1.5\% \pm 2\text{Hz}$				2,3,5,9	
6	Freq. deviation reject		$\pm 3.5\%$				2,3,5,9	
7	Third tone tolerance		-18.5			dB	2,3,4,5,9,13	
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10	
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11	

\*  $V_{DD}=5\text{V}$ ,  $V_{SS}=0$ ,  $T_A=25^\circ\text{C}$  and  $f_C=3.579545\text{MHz}$  using test circuit shown in Figure 2.

### NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by  $\pm 1.5\% \pm 2\text{Hz}$ .
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz)  $\pm 2\%$ .
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. For guard time calculation purposes.
13. Referenced to Fig. 10 Input DTMF Tone Level at -25 dBm (-28 dBm at GS Pin) Interference Frequency Range between 480-3400 Hz.

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AC Electrical Characteristics - - Voltages are with respect to ground (V<sub>SS</sub>) unless otherwise stated T-75-27-07

	Characteristics	Sym	Min	Typ <sup>†</sup>	Max	Units	Conditions
T I M I N G	Tone present detect time	t <sub>DP</sub>	5	11	14	ms	Note 12
	Tone absent detect time	t <sub>DA</sub>	0.5	4	8.5	ms	Note 12
	Tone duration accept	t <sub>REC</sub>			40	ms	User adjustable
	Tone duration reject	t <sub>REC</sub>	20			ms	User adjustable
	Interdigit pause accept	t <sub>ID</sub>			40	ms	User adjustable
	Interdigit pause reject	t <sub>DO</sub>	20			ms	User adjustable
O U T P U T S	Propagation delay (St to Q)	t <sub>PQ</sub>		8	11	μs	TOE = V <sub>DD</sub>
	Propagation delay (St to StD)	t <sub>PStD</sub>		12		μs	TOE = V <sub>DD</sub>
	Output data setup (Q to StD)	t <sub>QStD</sub>		3.4		μs	TOE = V <sub>DD</sub>
	Propagation delay (TOE to Q ENABLE)	t <sub>PTE</sub>		50		ns	R <sub>L</sub> = 10kΩ C <sub>L</sub> = 50 pF
	Propagation delay (TOE to Q DISABLE)	t <sub>PTD</sub>		300		ns	R <sub>L</sub> = 10kΩ C <sub>L</sub> = 50 pF
C L O C K	Crystal /clock frequency	f <sub>C</sub>	3.5759	3.5795	3.5831	MHz	
	Clock input rise time	t <sub>LHCL</sub>			110	ns	Ext. clock
	Clock input fall time	t <sub>HLCL</sub>			110	ns	Ext. clock
	Clock input duty cycle	DC <sub>CL</sub>	40	50	60	%	Ext. clock
	Capacitive load (OSC2)	C <sub>LO</sub>			30	pF	

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<sup>†</sup> V<sub>DD</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 25°C and f<sub>c</sub> = 3.579545 MHz, using test circuit shown in Figure 2.

<sup>‡</sup> Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

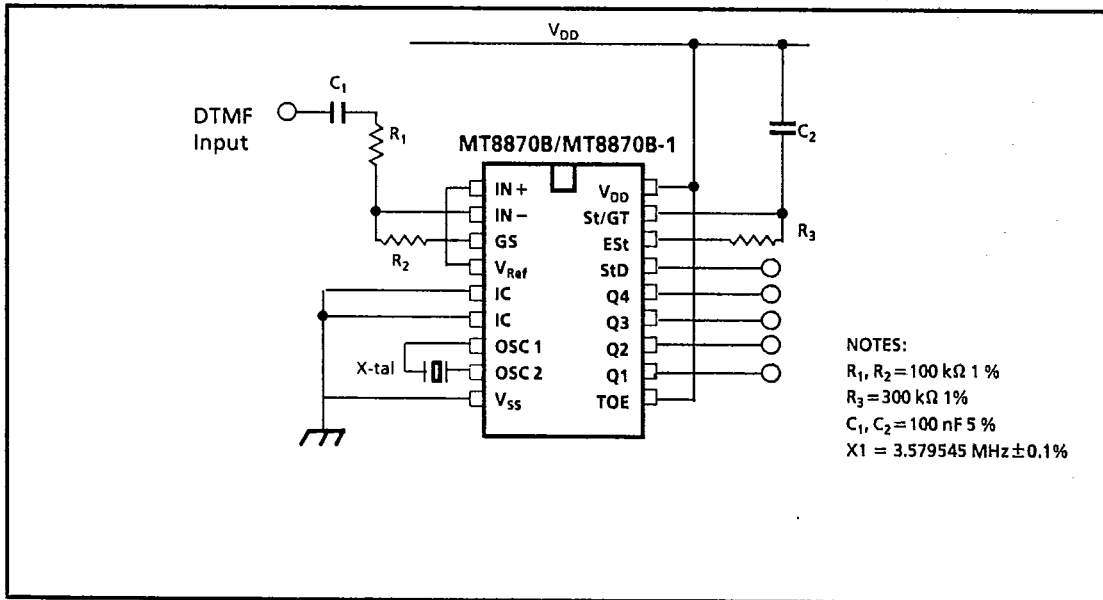


Figure 2 - Single-Ended Input Configuration

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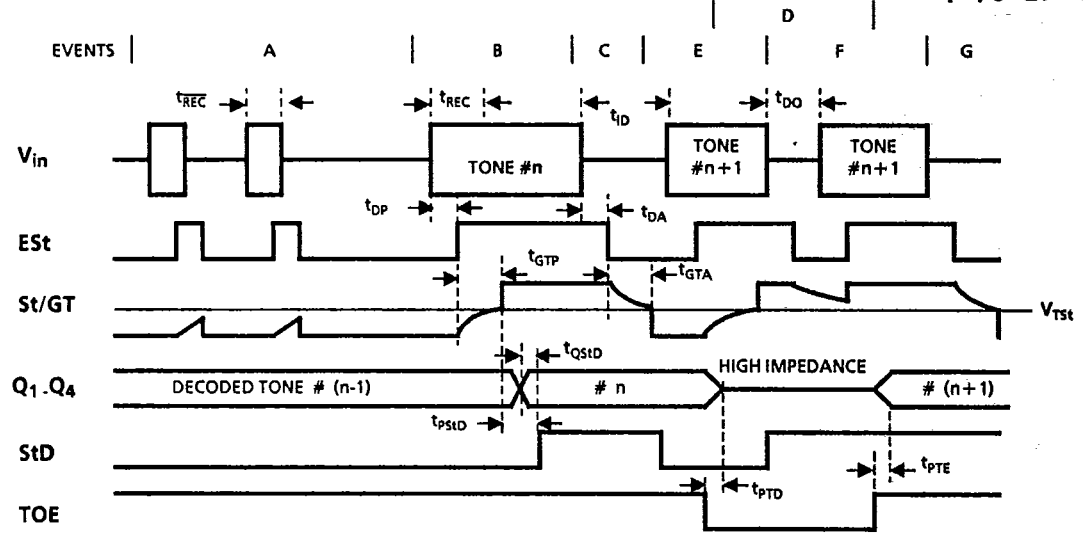
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## Pin Description

Pin #	Name	Description
1	IN +	Non-Inverting Op-Amp (Input).
2	IN -	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V <sub>Ref</sub>	Reference Voltage (Output), Nominally V <sub>DD</sub> /2 is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal Connection. Must be tied to V <sub>SS</sub> .
6	IC	Internal Connection. Must be tied to V <sub>SS</sub> .
7	OSC1	Clock (Input).
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V <sub>SS</sub>	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V <sub>TSt</sub> .
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V <sub>TSt</sub> detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V <sub>TSt</sub> frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V <sub>DD</sub>	Positive power supply (Input).



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**EXPLANATION OF EVENTS**

- A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.
- B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.
- C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.
- D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.
- E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).
- F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.
- G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

**EXPLANATION OF SYMBOLS**

- V<sub>in</sub> DTMF COMPOSITE INPUT SIGNAL.
- ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
- St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
- Q<sub>1</sub>-Q<sub>4</sub> 4-BIT DECODED TONE OUTPUT.
- StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.
- TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q<sub>1</sub>-Q<sub>4</sub> TO ITS HIGH IMPEDANCE STATE.
- $t_{REC}$  MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
- $t_{REC}$  MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
- $t_{ID}$  MINIMUM TIME BETWEEN VALID DTMF SIGNALS.
- $t_{DO}$  MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
- $t_{DP}$  TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
- $t_{DA}$  TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
- $t_{GTP}$  GUARD TIME, TONE PRESENT.
- $t_{GTA}$  GUARD TIME, TONE ABSENT.

Figure 3- Timing Diagram

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## Functional Description

The MT8870B/MT8870B-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

### Filter Section

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

### Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone

simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

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### Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes  $v_c$  (see Figure 5) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period ( $t_{GTP}$ ),  $v_c$  reaches the threshold ( $V_{TS}$ ) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives  $v_c$  to  $V_{DD}$ . GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit

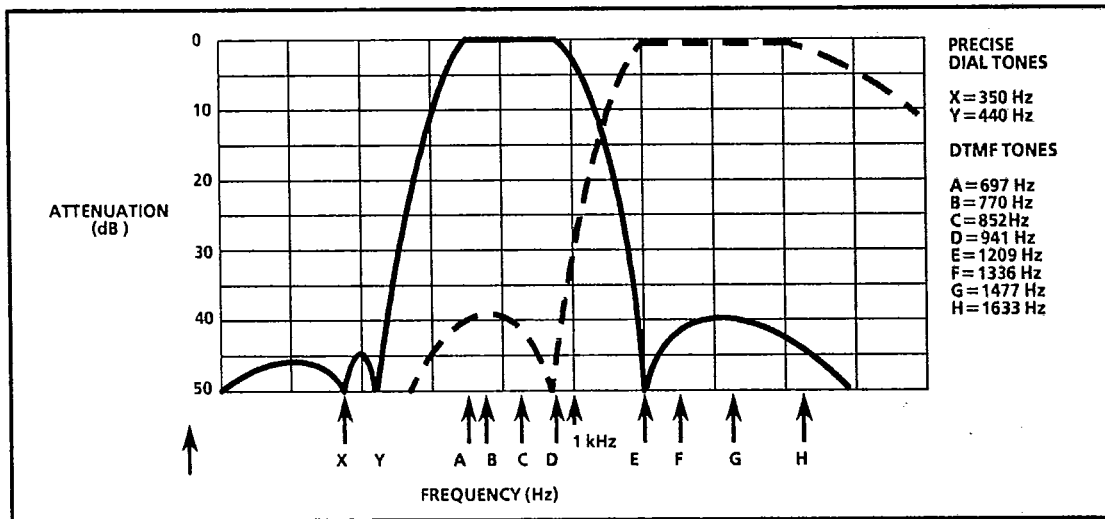


Figure 4- Filter Response



recommended for most applications, leaving R to be selected by the designer.

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F <sub>LOW</sub>	F <sub>HIGH</sub>	NO.	TOE	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Table 1. Functional Decode Table

pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

**Guard Time Adjustment**

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 5 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of  $t_{DP}$  is a device parameter (see Figure 3) and  $t_{REC}$  is the minimum signal duration to be recognized by the receiver. A value for C of 0.1  $\mu$ F is

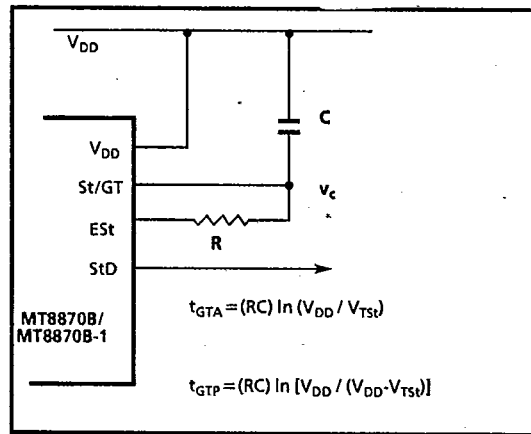


Figure 5- Basic Steering Circuit

Different steering arrangements may be used to select independently the guard times for tone present ( $t_{GTP}$ ) and tone absent ( $t_{GTA}$ ). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing  $t_{REC}$  improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short  $t_{REC}$  with a long  $t_{DO}$  would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone dropouts are required. Design information for guard time adjustment is shown in Figure 6.

**Differential Input Configuration**

The input arrangement of the MT8870B/MT8870B-1 provides a differential-input operational amplifier as well as a bias source ( $V_{Ref}$ ) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (G5) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 2 with the op-amp connected for unity gain and  $V_{Ref}$  biasing the input at  $\frac{1}{2}V_{DD}$ . Figure 7 shows the differential configuration, which permits the adjustment of gain with the feedback resistor  $R_5$ .

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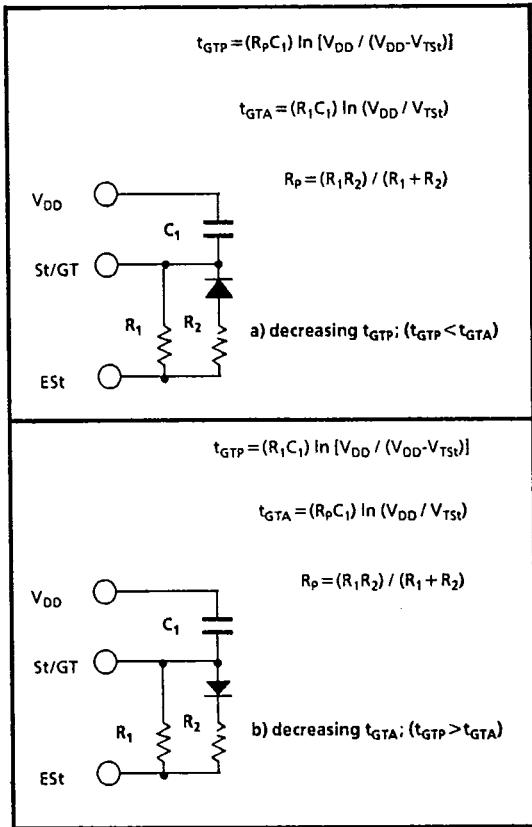


Figure 6- Guard Time Adjustment

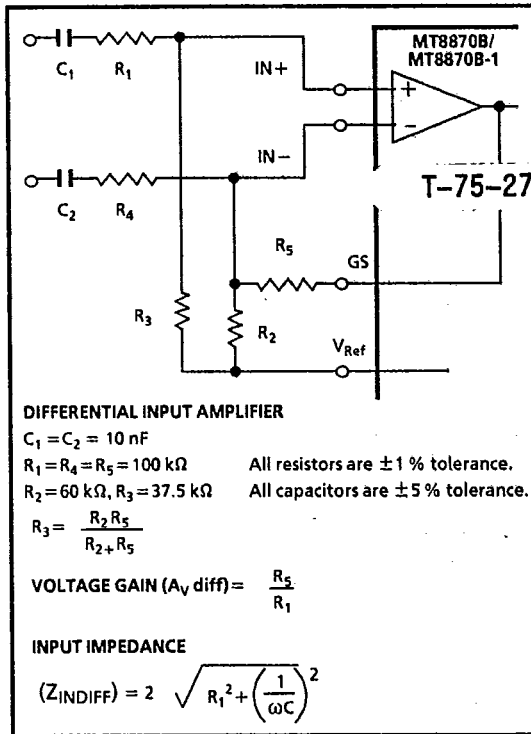


Figure 7- Differential Input Configuration

**Crystal Oscillator**

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870B/MT8870B-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 8 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

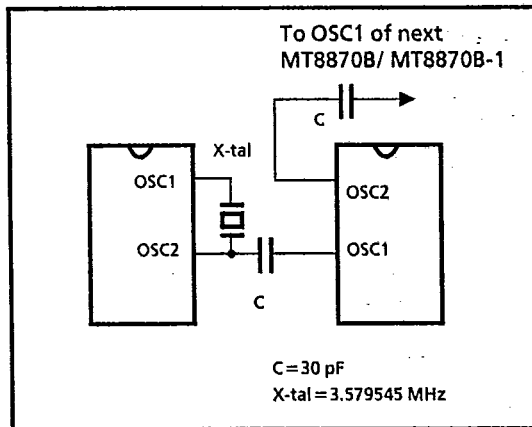


Figure 8- Oscillator Connection

APPLICATION

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 10 illustrates the use of MT8870B-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R<sub>1</sub> and R<sub>2</sub> to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870B-1. As shown in the diagram, the component values of R<sub>3</sub> and C<sub>2</sub> are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 9.

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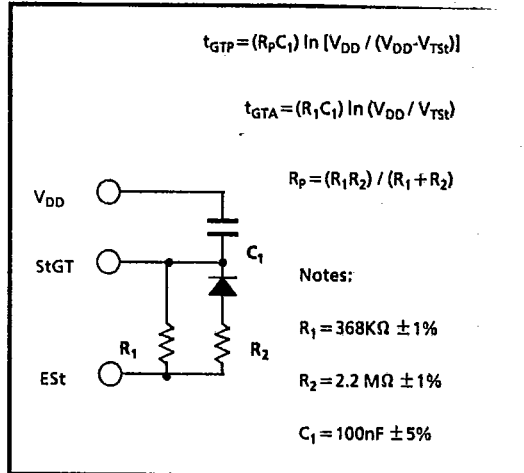


Figure 9 - Non-Symmetric Guard Time Circuit

3

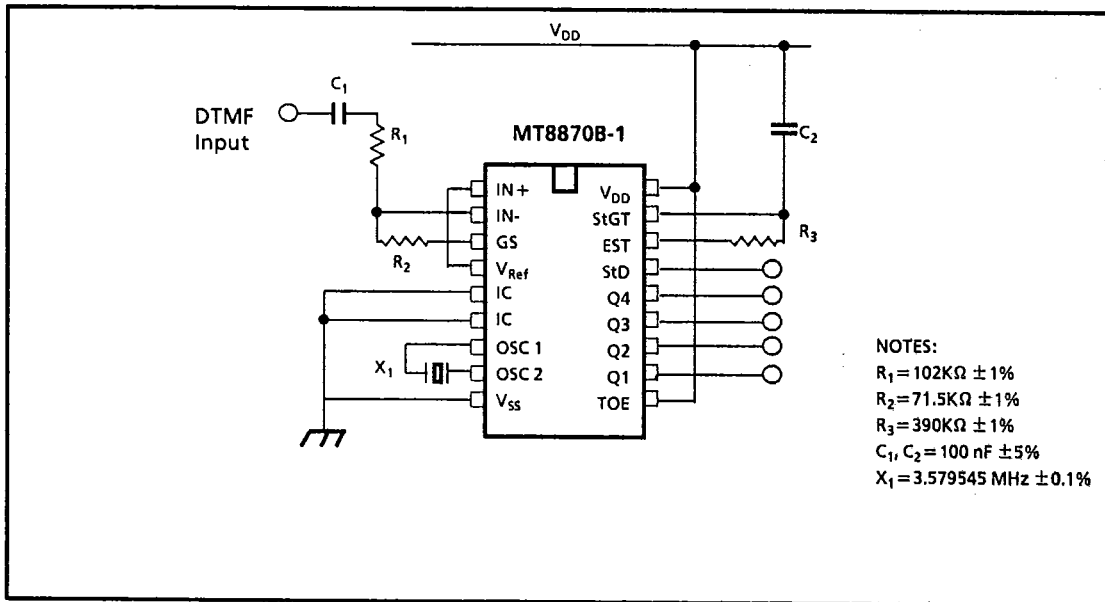
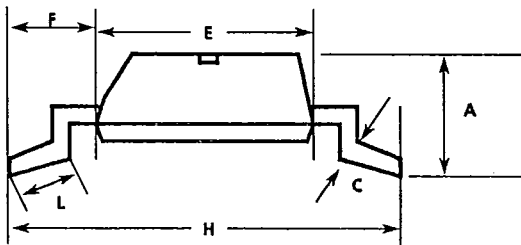
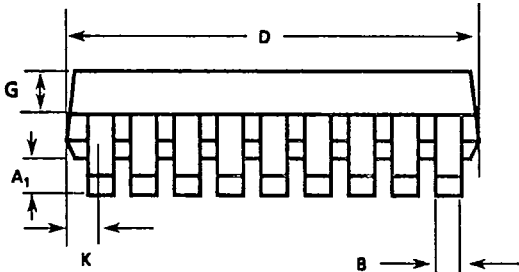
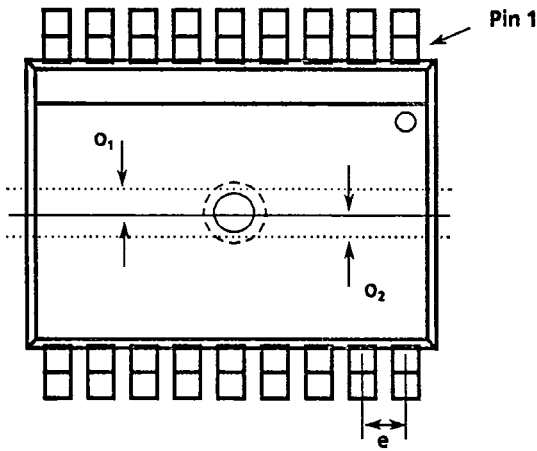


Figure 10 - Single-Ended Input Configuration for BT or CEPT Spec

T-90-20



DIM	18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A <sub>1</sub>	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
K	0.035 (0.889)	0.045 (1.143)	0.035 (0.889)	0.045 (1.143)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
O <sub>1</sub>	-	0.005 (0.13)	-	0.005 (0.13)
O <sub>2</sub>	-	0.005 (0.13)	-	0.005 (0.13)

NOTE: ( ) millimeters

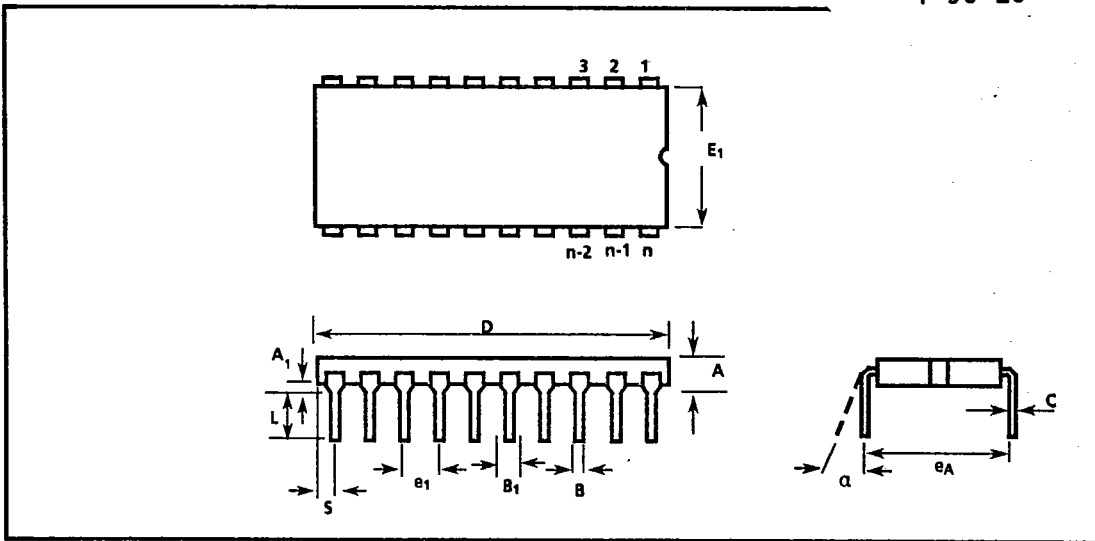
**NOTES:**

- 1) A & B Maximum dimensions include allowable mold flash.
- 2) O<sub>1</sub> & O<sub>2</sub> are SYMMETRY dimensions.

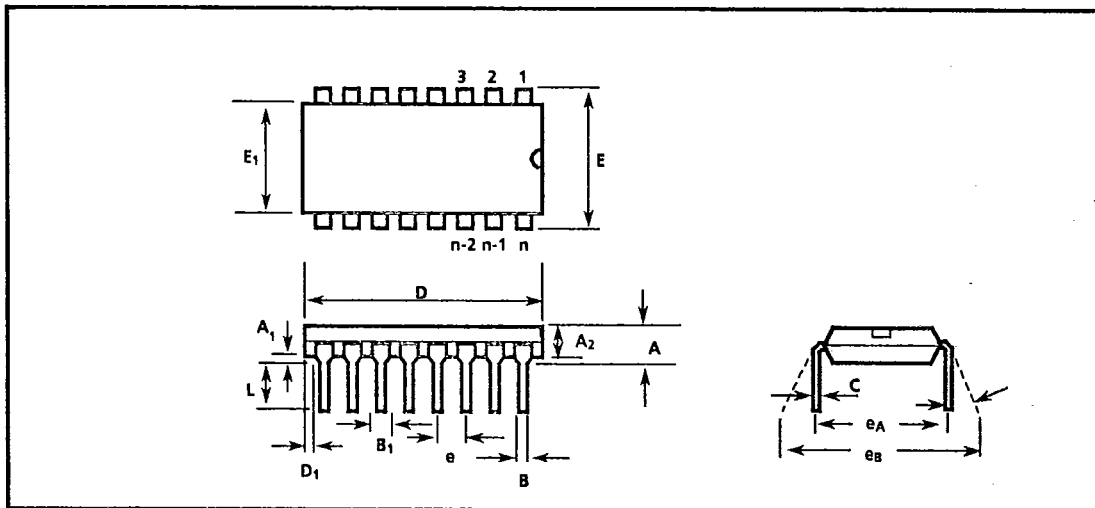
Lead SOIC Package (S Suffix)

Package Outlines

T-90-20



Ceramic Dual-In-Line Packages (CDIP) - C Suffix



Plastic Dual-In-Line Packages (PDIP) - E Suffix

Package Outlines

T-90-20

DIM	8-Pin				16-Pin				18-Pin				20-Pin				
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)	
A <sub>1</sub>			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)	
A <sub>2</sub>	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	
B <sub>1</sub>	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)			0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.930 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D <sub>1</sub>	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)					0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			
E <sub>1</sub>	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				
e <sub>1</sub>			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)		
eA	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		
eB		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)			
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)	
α			0°	15°			0°	15°			0°	15°			0°	15°	

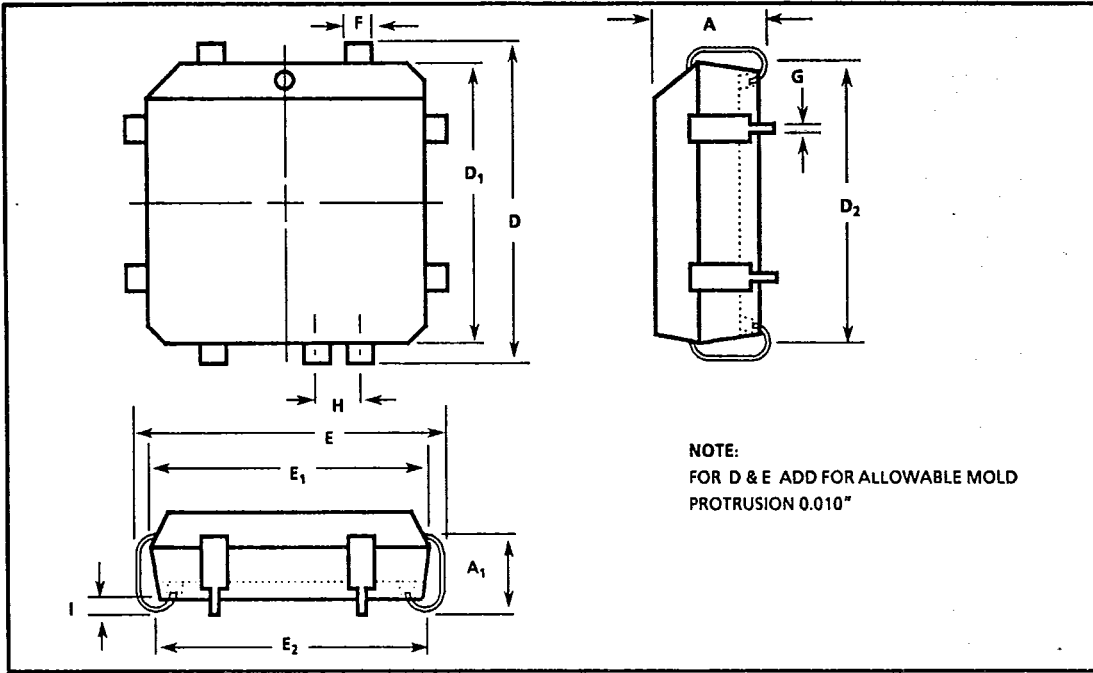
NOTE: ( ) Millimeters

## Package Outlines

T-90-20

DIM	22-Pin				24-Pin				28-Pin				40-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A <sub>1</sub>			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A <sub>2</sub>	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B <sub>1</sub>	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D <sub>1</sub>	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E <sub>1</sub>	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.11)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e <sub>1</sub>			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
eA	0.400 BSC (10.16 BSC)		0.400 BSC (10.16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
eB		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters



Plastic J-Lead Chip Carrier (P-Suffix)



# Package Outlines

MITEL SEMICONDUCTOR

35E D ■ 6249370 0005783 T ■ MITC

T-90-20



DIM	20-Pin		28-Pin		44-Pin		68-Pin		84-Pin	
	PLCC		PLCC		PLCC		PLCC		PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A <sub>1</sub>	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.511 TP)							
B <sub>1</sub>										
B <sub>2</sub>										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	0.185 (30.10)	1.195 (30.35)
D <sub>1</sub> /E <sub>1</sub>	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D <sub>2</sub> /E <sub>2</sub>	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D <sub>4</sub> /E <sub>4</sub>										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h			0.040 BSC (1.02 BSC)							
h <sub>1</sub>										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L <sub>1</sub>										
R <sub>1</sub>										

NOTE: ( ) Millimeters