OKI semiconductor

MSM41256A

262,144-WORD x 1-BIT DYNAMIC RAM <PAGE MODE TYPE>

GENERAL DESCRIPTION

The Oki MSM41256A is a fully decoded, dynamic NMOS random access memory organized as 262,144-word x 1 bit. The design is optimized for high-speed, high-performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low-power dissipation and compact layout are required.

Multiplexed row and column address input permits MSM41256A housing in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41256A offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh capability.

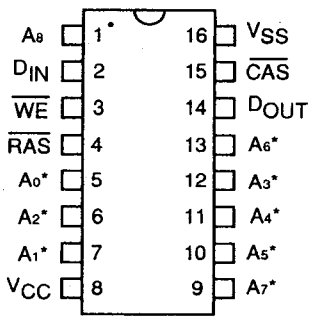
The MSM41256A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry, including the sense amplifiers, is employed in the design.

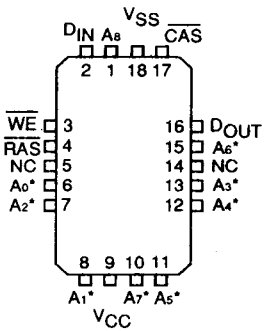
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262,144 x 1 RAM, 16 or 18 pin package
- Silicon-gate, double-poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41256A-10)
  - 120 ns max (MSM41256A-12)
  - 150 ns max (MSM41256A-15)
- Cycle time:
  - 200 ns min (MSM41256A-10)
  - 220 ns min (MSM41256A-12)
  - 260 ns min (MSM41256A-15)
- Low power:
  - 330 mW active (MSM41256A-10)
  - 303 mW active (MSM41256A-12)
  - 275 mW active (MSM41256A-15)
  - 28 mW max standby
- Single +5V power supply, ±10% tolerance
- All inputs are TTL compatible, low-capacitive load
- Three-state TTL compatible output
- Gated $\overline{CAS}$
- 256 refresh cycles/4 ms
- Common I/O capability using Early Write operation
- Output unlatched at cycle end to allow extended page boundary and two-dimensional chip select
- Read-Modify-Write and $\overline{RAS}$-only refresh, capability
- On-chip latches for addresses and data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- Page Mode capability

PIN CONFIGURATION (TOP VIEW)

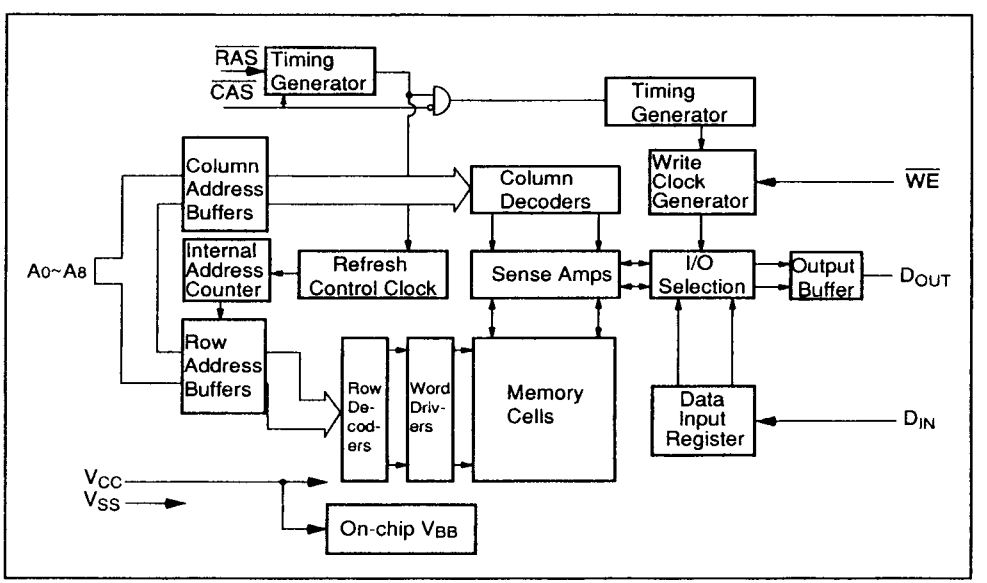




* Refresh Address

Pin Names	Function
A0 ~ A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Adress Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Condition	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	–	-1 to +7	V
Operating temperature	T_{opr}	–	0 to 70	°C
Storage temperature	T_{stg}	–	-55 to +150	°C
Power dissipation	P_D	–	1.0	W
Short circuit output current	–	–	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Condition	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply voltage	V_{CC}	–	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	–	0	0	0	V	
Input high voltage, all inputs	V_{IH}	–	2.4	–	6.5	V	
Input low voltage, all inputs	V_{IL}	–	−1.0	–	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Condition	MSM41256A			Unit	Notes
				Min.	Typ.	Max.		
OPERATING CURRENT* Average power suply current (RAS, CAS cycling; t_{RC} = min.)	MSM41256A-10	I_{CC1}	–	–	–	60	mA	
	MSM41256A-12					55		
	MSM41256A-15					50		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	–	–	–	5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256A-10	I_{CC3}	–	–	–	55	mA	
	MSM41256A-12					50		
	MSM41256A-15					45		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256A-10	I_{CC4}	–	–	–	40	mA	
	MSM41256A-12					35		
	MSM41256A-15					30		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before, $\overline{RAS}$; t_{RC} = min.)	MSM41256A-10	I_{CC5}	–	–	–	55	mA	
	MSM41256A-12					50		
	MSM41256A-15					45		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	–	–10	–	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	–	–10	–	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = –5 mA)		V_{OH}	–	2.4	–		V	
Output low volage (I_{OL} = 4.2 mA)		V_{OL}				0.4	V	

Note*: ICC depends on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Input capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

* Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	Symbol	MSM41256A -10		MSM41256A -12		MSM41256A -15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	4	–	4	–	4	ms	–
Random read or write cycle time	t_{RC}	200	–	220	–	260	–	ns	–
Read-write cycle time	t_{RWC}	205	–	225	–	260	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	4,5
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	4,5
Output buffer turn-off delay	t_{OFF}	0	30	0	30	0	30	ns	–
Transition time	t_T	3	50	3	50	3	50	ns	–
$\overline{RAS}$ precharge time	t_{RP}	90	–	90	–	100	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	75	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	–
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	20	–	25	–	30	–	ns	–
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row address hold time	t_{RAH}	15	–	15	–	15	–	ns	–
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	–
Column address hold time	t_{CAH}	20	–	20	–	25	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	7
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20	–	20	–	20	–	ns	7
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	6

AC CHARACTERISTICS (CONT.)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSM41256A -10		MSM41256A -12		MSM41256A -15		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write command pulse width	t_{WP}	15	–	20	–	25	–	ns	–
Write command hold width	t_{WCH}	15	–	20	–	25	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	35	–	40	–	45	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	35	–	40	–	45	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	–
Data-in hold time	t_{DH}	20	–	20	–	25	–	ns	–
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	15	–	20	–	25	–	ns	6
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	20	–	25	–	30	–	ns	–
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	20	–	25	–	30	–	ns	–
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	20	–	25	–	30	–	ns	–
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20	–	20	–	20	–	ns	–
Page mode cycle time	t_{PC}	100	–	120	–	145	–	ns	–
Page mode read write cycle time	t_{PRWC}	105	–	125	–	145	–	ns	–
Page mode $\overline{CAS}$ precharge time	t_{CP}	40	–	50	–	60	–	ns	–
Refresh counter test cycle time	t_{RTC}	315	–	355	–	415	–	ns	–
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	215	10,000	255	10,000	305	10,000	ns	–
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50	–	60	–	70	–	ns	–

Notes: 1 An initial pause of 100 μs is required after power-up followed by a minimum of any eight $\overline{RAS}$ cycles (example: $\overline{RAS}$ only Refresh) before proper device operation is achieved.

2 The AC measurements assume the transition time (t_T) = 5 ns.

3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

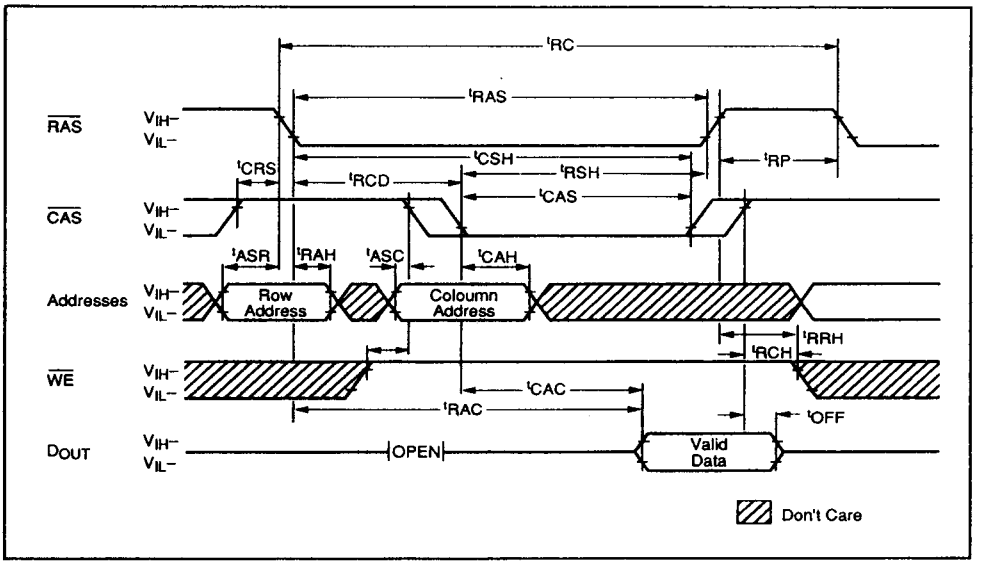
4 Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then the access time will be controlled exclusively by t_{CAC}.

5 Measured using an equivalent load circuit of 2 TTL loads and 100 pF.

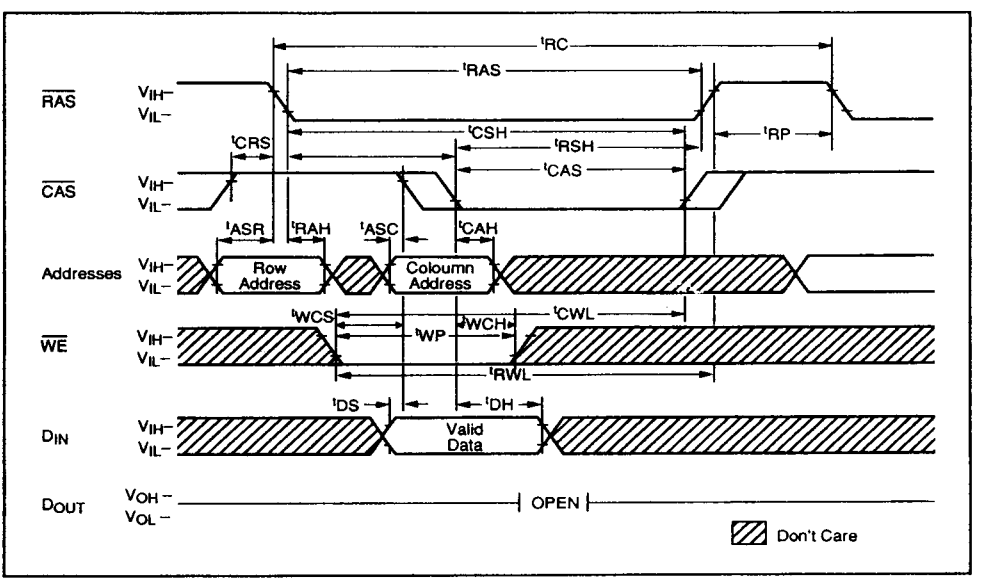
6 The specs t_{WCS}, t_{RWD}, and t_{CWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.) then the cycle is an "Early Write" cycle and the data out will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) then the cycle is a "Read-Write" cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied then the condition of data out will be indeterminate at access time.

7 Either the t_{RRH} or the t_{RCH} spec. must be satified for a proper read cycle.

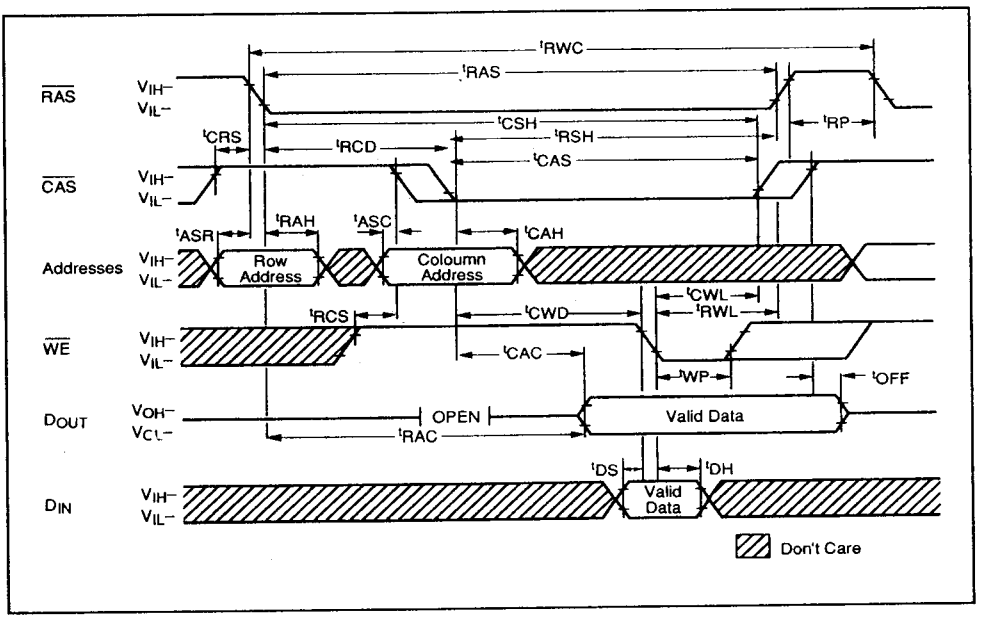
READ CYCLE



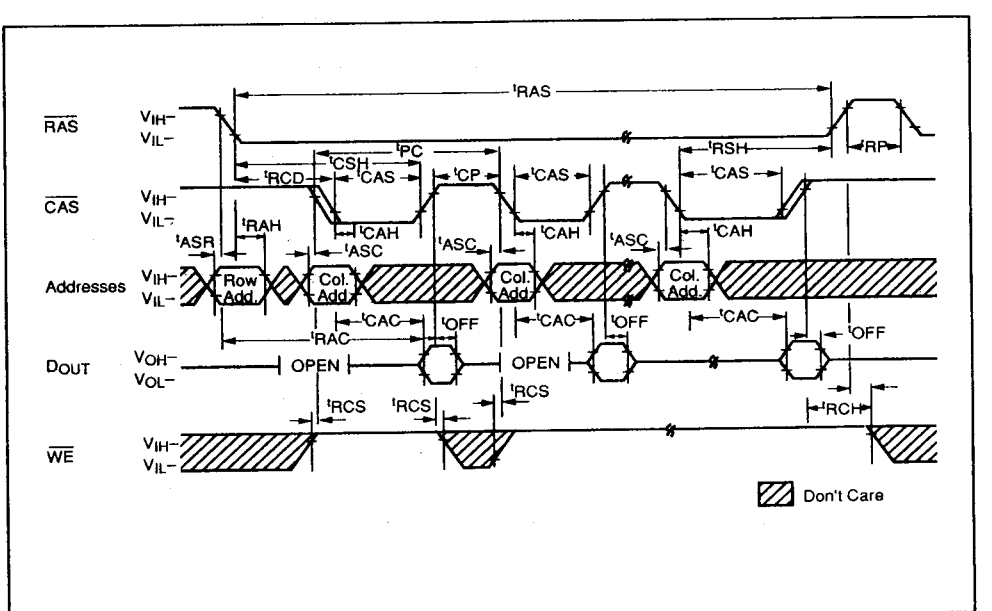
WRITE CYCLE (EARLY WRITE)



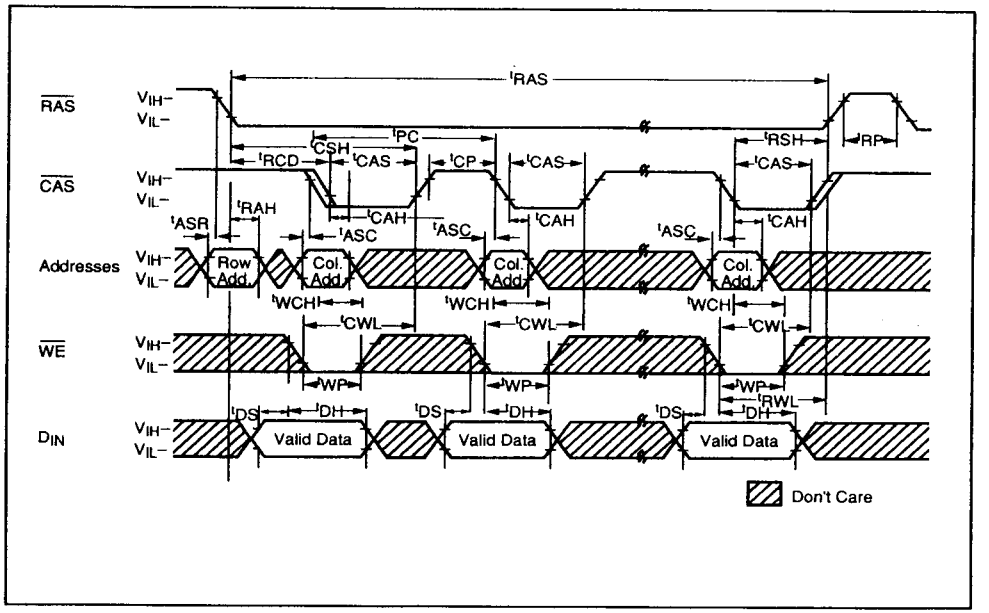
READ WRITE/READ-MODIFIY-WRITE CYCLE



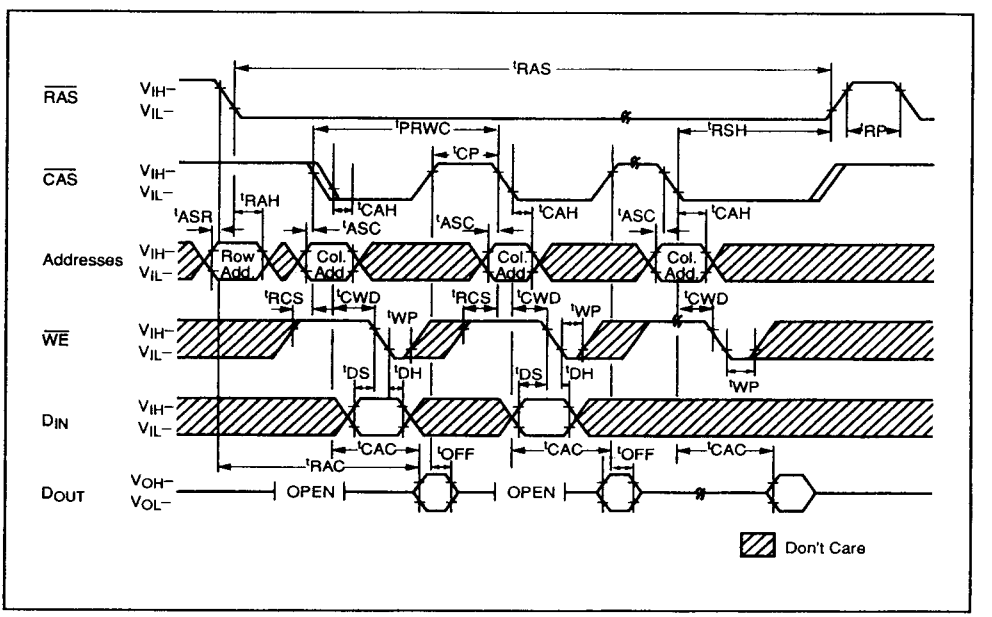
PAGE MODE READ CYCLE



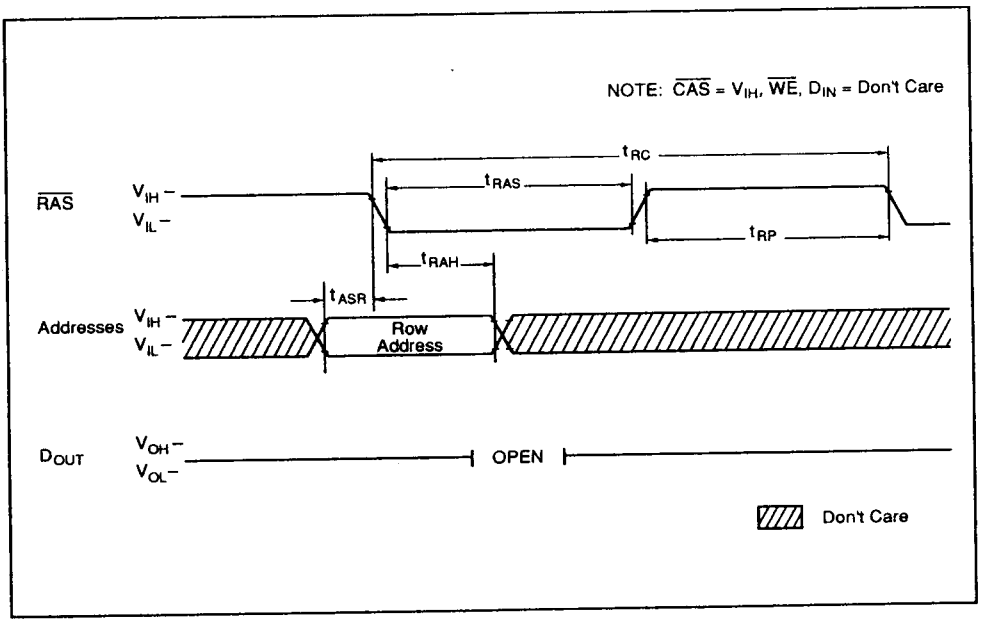
PAGE MODE WRITE CYCLE



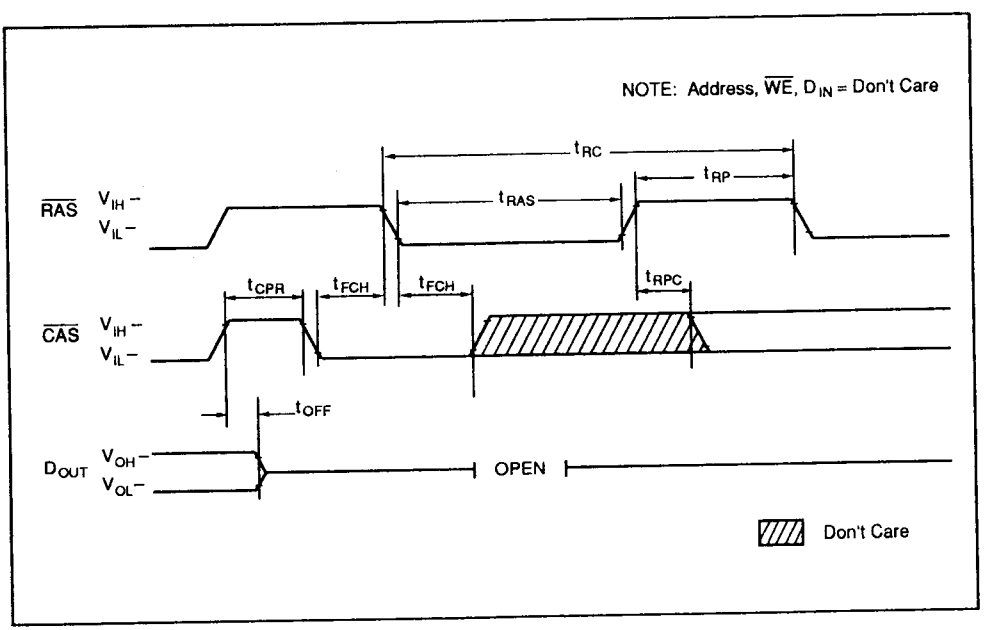
PAGE MODE READ-MODIFY-WRITE CYCLE



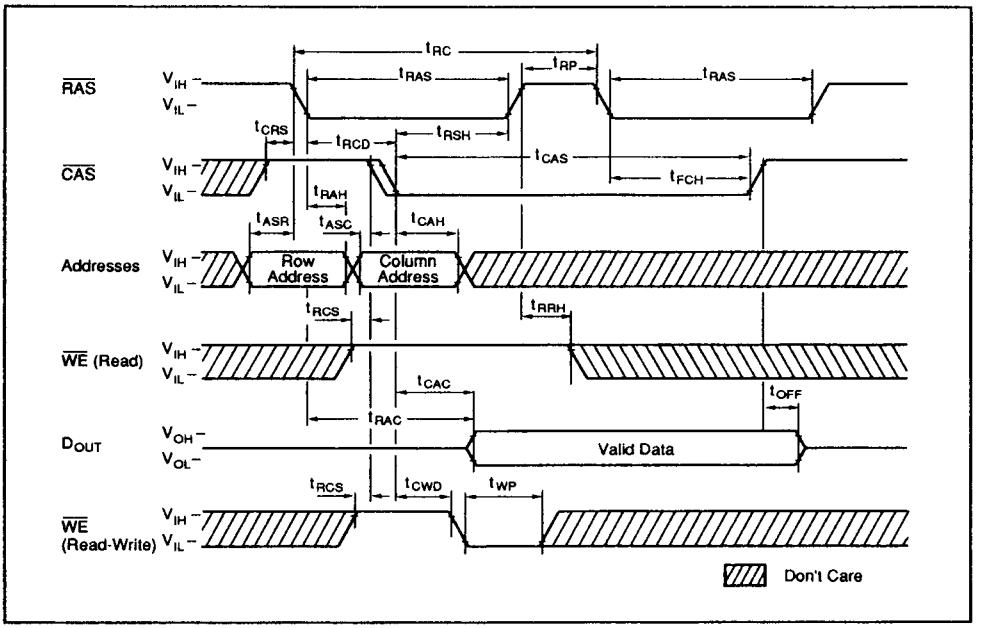
$\overline{RAS}$-ONLY REFRESH CYCLE



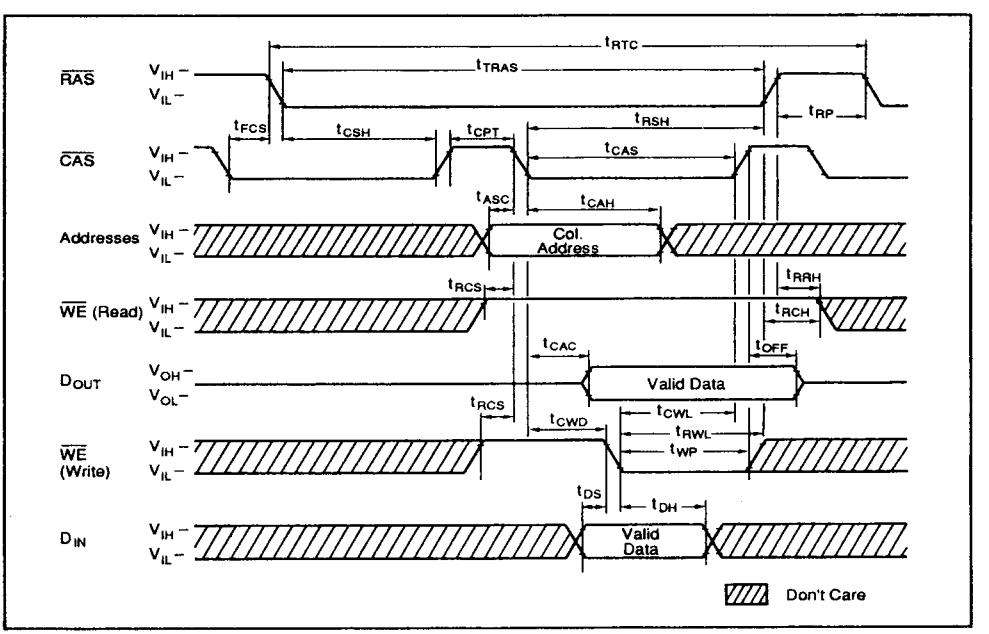
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



MSM41256A BIT MAP (PHYSICAL-DECIMAL)

252	253	254	255		3	2	1	0
128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0
384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0
129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0
385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0
254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0
510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0
255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0
511	511	511	511		511	511	511	511

COLUMN DECODER

256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128
256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384
256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129
256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385
256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254
256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510
256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255
256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0
383	383	383	383		383	383	383	383
252	253	254	255		3	2	1	0
127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0
382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0
126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0
257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0
1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0
256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0
0	0	0	0		0	0	0	0

COLUMN DECODER

256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383
256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127
256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382
256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126
256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257
256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1
256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256
256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0

A8 ROW = LOW
REFRESH ADDRESS
(0–255)

A8 ROW = HIGH
REFRESH ADDRESS
(0–255)

□ Pin8

A
B
:CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

ROW ADDRESS	COLUMN ADDRESS	
8N+6, 8N+7, 8N, 8N+1	2N	:POSITIVE
8N+2,8N+3, 8N+4, 8N+5	2N	:NEGATIVE
8N+6, 8N+7, 8N, 8N+1	2N+1	:NEGATIVE
8N+2, 8N+3, 8N+4, 8N+5	2N+1	:POSITIVE
N=0, 1, 2,.....63	N=0, 1, 2,.....255	