MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

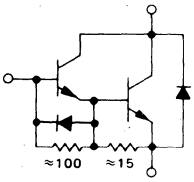
MJ10006
MJ10007

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
30 ns Inductive Fall Time – 25°C (Typ)
500 ns Inductive Storage Time – 25°C (Typ))
Operating Temperature Range -65 to +200°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

10 AMPERE

NPN SILICON

POWER DARLINGTON TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

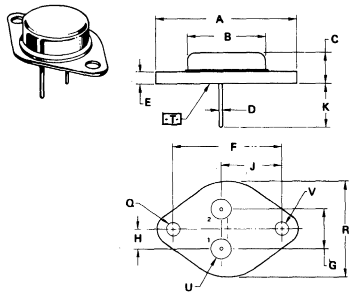
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEX}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
| ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS:
| ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10006		350	–	–	
	MJ10007		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10006		400	–	–	
	MJ10007		450	–	–	
(I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10006		275	–	–	
	MJ10007		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)			40	–	500	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 250 mAdc)			–	–	1.9	
(I_C = 10 Adc, I_B = 1.0 Adc)			–	–	2.9	
(I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5.0 Adc, I_B = 250 mAdc)			–	–	2.5	
(I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 5.0 Adc)		V_f	–	3.0	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.25	0.6	μs
Storage Time		t_s	–	0.5	1.5	μs
Fall Time		t_f	–	0.06	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	0.8	2.0	μs
Crossover Time		t_c	–	0.6	1.5	μs
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.5	–	μs
Crossover Time		t_c	–	0.3	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

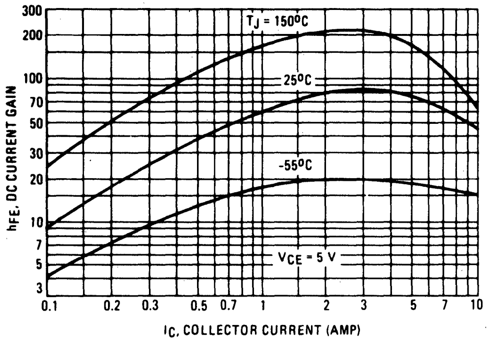


FIGURE 2 – COLLECTOR SATURATION REGION

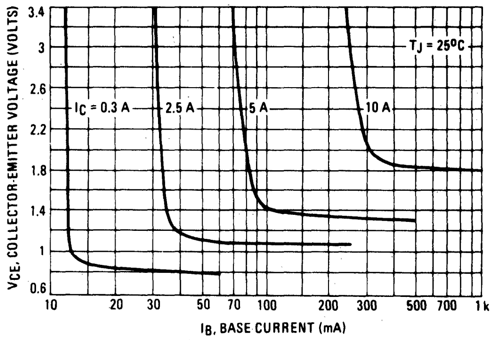


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

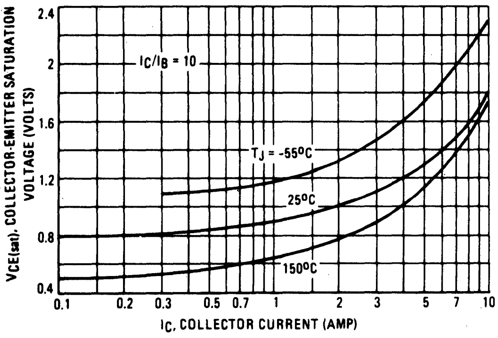


FIGURE 4 – BASE-EMITTER VOLTAGE

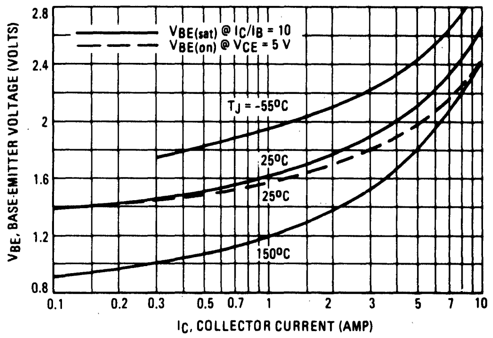


FIGURE 5 – COLLECTOR CUTOFF REGION

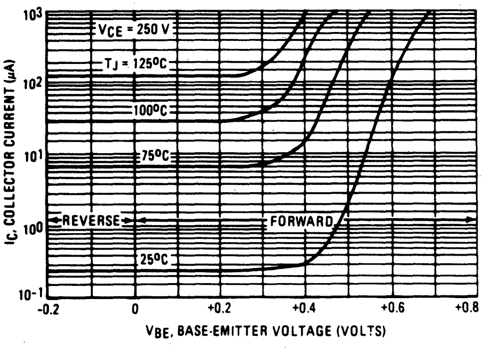


FIGURE 6 – OUTPUT CAPACITANCE

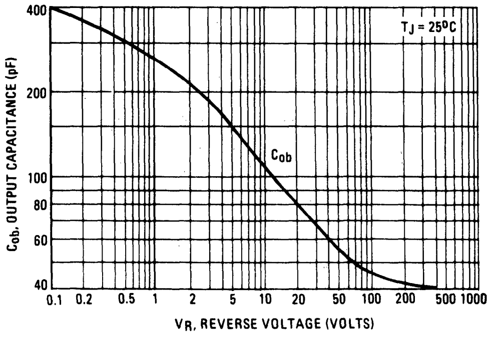


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

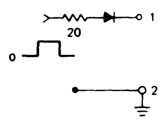
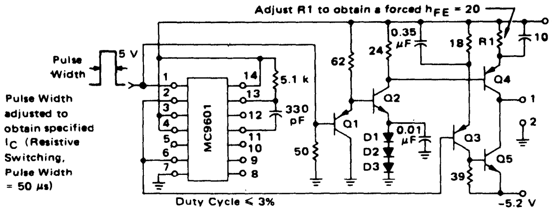
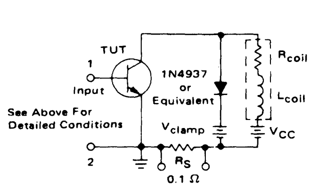
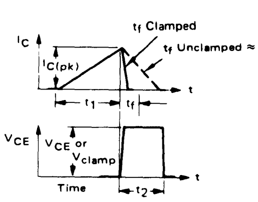
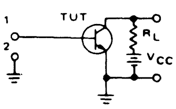
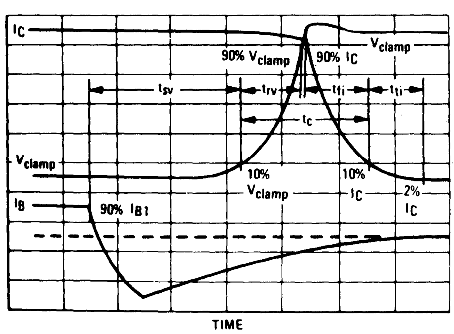
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA		Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equipment	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

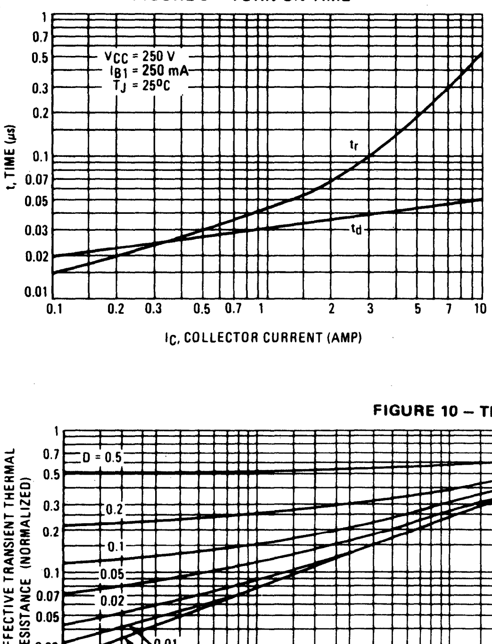


FIGURE 9 – TURN-OFF TIME

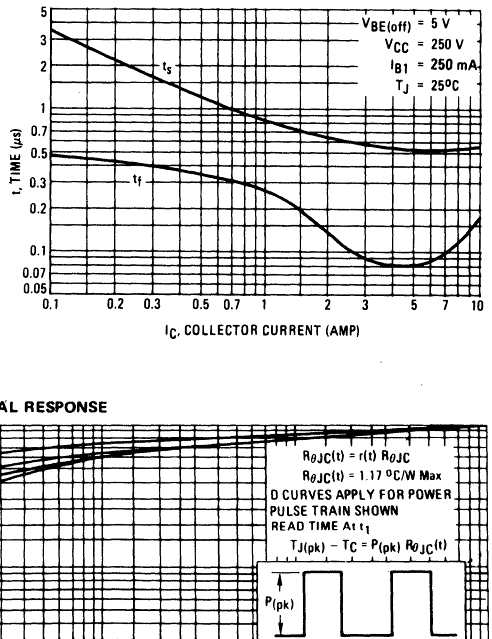


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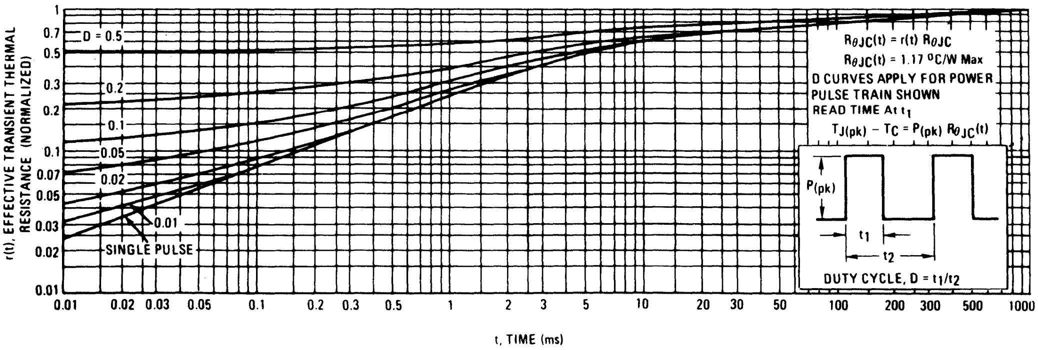
FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

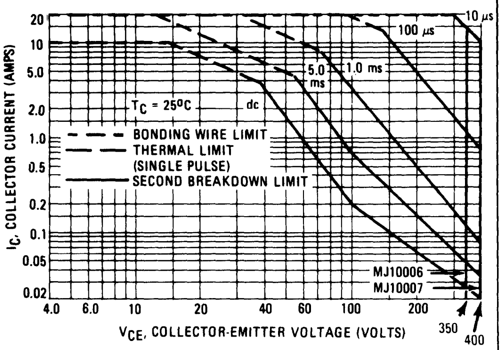
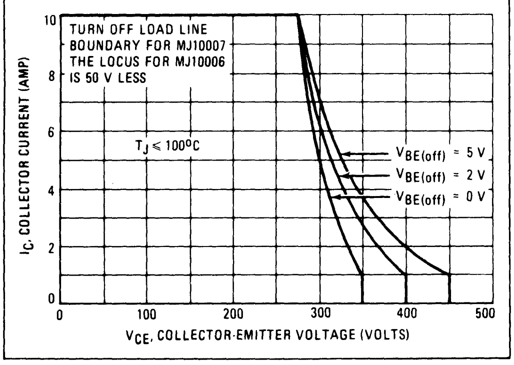


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

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FIGURE 13 — POWER DERATING