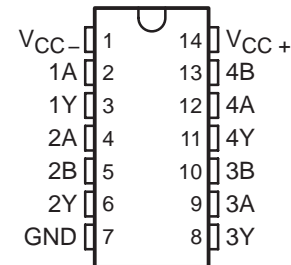- **Meet or Exceed the Requirements of ANSI TIA/EIA-232-E and ITU Recommendation V.28**
- **Current-Limited Output: 10 mA Typical**
- **Power-Off Output Impedance: 300 Ω Minimum**
- **Slew Rate Control by Load Capacitor**
- **Flexible Supply-Voltage Range**
- **Input Compatible With Most TTL Circuits**
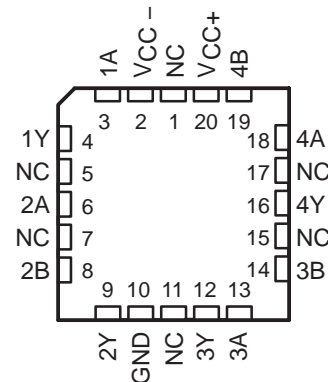
description/ordering information

The MC1488, SN55188, and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with ANSI TIA/EIA-232-E, using a diode in series with each supply-voltage terminal as shown under typical applications.

The SN55188 is characterized for operation over the full military temperature range of −55°C to 125°C. The MC1488 and SN75188 are characterized for operation from 0°C to 70°C.

SN55188 . . . J OR W PACKAGE
SN75188 . . . D, N, OR NS PACKAGE
MC1488 . . . N PACKAGE
(TOP VIEW)

V_{CC-}	1		14	V_{CC+}
1A	2		13	4B
1Y	3		12	4A
2A	4		11	4Y
2B	5		10	3B
2Y	6		9	3A
GND	7		8	3Y

SN55188 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1A (3), V_{CC-} (2), NC (1), V_{CC+} (20), 4B (19)

1Y	4		18	4A
NC	5		17	NC
2A	6		16	4Y
NC	7		15	NC
2B	8		14	3B

Bottom pins: 2Y (9), GND (10), NC (11), 3Y (12), 3A (13)

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MC1488N	MC1488N
		Tube of 25	SN75188N	SN75188N
	SOIC (D)	Tube of 50	SN75188D	SN75188
		Reel of 2500	SN75188DR	
	SOP (NS)	Reel of 2000	SN75188NSR	SN75188
−55°C to 125°C	CDIP (J)	Tube of 25	SN55188J	SN55188J
			SNJ55188J	SNJ55188J
	CFP (W)	Tube of 150	SNJ55188W	SNJ55188W
	LCCC (FK)	Tube of 55	SNJ55188FK	SNJ55188FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

MC1488, SN55188, SN75188
QUADRUPLE LINE DRIVERS

FUNCTION TABLE
(drivers 2–4)

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

logic diagram (positive logic)
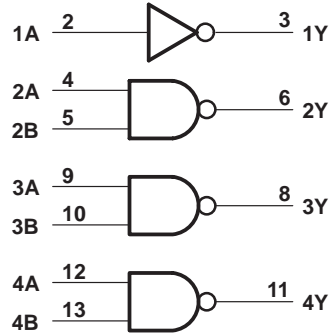
Positive logic
Y = $\overline{A}$ (driver 1)
Y = $\overline{AB}$ or $\overline{A}$ + $\overline{B}$ (drivers 2 thru 4)

schematic (each driver)
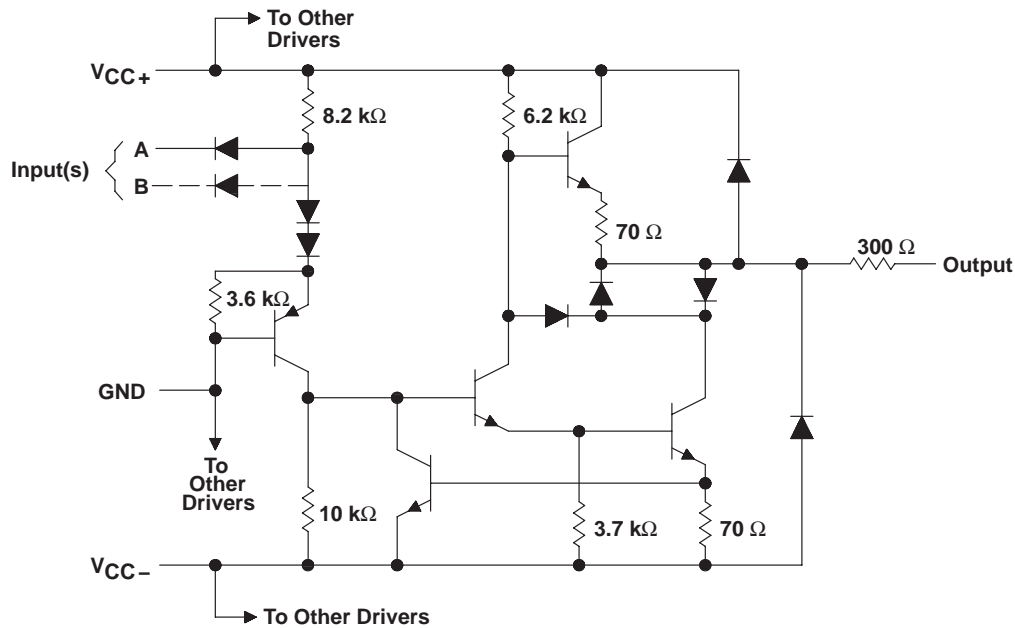
Resistor values shown are nominal.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . 15 V
Supply voltage, V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . −15 V
Input voltage, V_I . . . . −15 V to 7 V
Output voltage, V_O . . . . −15 V to 15 V
Continuous total power dissipation (see Note 2) . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package . . . . 86°C/W
                                                              N package . . . . 80°C/W
                                                              NS package . . . . 76°C/W
Operating virtual junction temperature, T_J . . . . 150°C
Case temperature for 60 seconds, FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . 300°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to the network ground terminal.
        2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the J package, SN55188
           chips are alloy mounted.
        3. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable
           ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
        4. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		SN55188			MC1488, SN75188			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC+}	Supply voltage	7.5	9	15	7.5	9	15	V
V_{CC-}	Supply voltage	−7.5	−9	−15	−7.5	−9	−15	V
V_{IH}	High-level input voltage	1.9			1.9			V
V_{IL}	Low-level input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm9$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188			MC1488, SN75188			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	$V_{IL} = 0.8$ V, $R_L = 3$ kΩ	$V_{CC+} = 9$ V, $V_{CC-} = -9$ V	6	7		6	7		V
			$V_{CC+} = 13.2$ V, $V_{CC-} = -13.2$ V	9	10.5		9	10.5		
V_{OL}	Low-level output voltage	$V_{IH} = 1.9$ V, $R_L = 3$ kΩ	$V_{CC+} = 9$ V, $V_{CC-} = -9$ V		-7‡	-6		-7	-6	V
			$V_{CC+} = 13.2$ V, $V_{CC-} = -13.2$ V		-10.5‡	-9		-10.5	-9	
I_{IH}	High-level input current	$V_I = 5$ V				10			10	µA
I_{IL}	Low-level input current	$V_I = 0$			-1	-1.6		-1	-1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level§	$V_I = 0.8$ V,	$V_O = 0$	-4.6	-9	-13.5	-6	-9	-12	mA
$I_{OS(L)}$	Short-circuit output current at low level§	$V_I = 1.9$ V,	$V_O = 0$	4.6	9	13.5	6	9	12	mA
r_O	Output resistance, power off	$V_{CC+} = 0$, $V_O = -2$ V to 2 V	$V_{CC-} = 0$,	300			300			Ω
I_{CC+}	Supply current from V_{CC+}	$V_{CC+} = 9$ V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		$V_{CC+} = 12$ V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		$V_{CC+} = 15$ V, No load, $T_A = 25°$C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I_{CC-}	Supply current from I_{CC-}	$V_{CC-} = -9$ V, No load	All inputs at 1.9 V		-13	-17		-13	-17	mA
			All inputs at 0.8 V			-0.5			-0.015	
		$V_{CC-} = -12$ V, No load	All inputs at 1.9 V		-18	-23		-18	-23	
			All inputs at 0.8 V			-0.5			-0.015	
		$V_{CC-} = -15$ V, No load, $T_A = 25°$C	All inputs at 1.9 V			-34			-34	
			All inputs at 0.8 V			-2.5			-2.5	
P_D	Total power dissipation	$V_{CC+} = 9$ V, No load	$V_{CC-} = -9$ V,			333			333	mW
		$V_{CC+} = 12$ V, No load	$V_{CC-} = -12$ V,			576			576	

† All typical values are at $T_A = 25°$C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if -6 V is a maximum, the typical value is a more negative voltage.

§ Not more than one output should be shorted at a time.

![Texas Instruments logo]

switching characteristics, $V_{CC\pm} = \pm 9$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output				220	350	ns
t_{PHL}	Propagation delay time, high- to low-level output	$R_L = 3$ kΩ,	$C_L = 15$ pF,		100	175	ns
t_{TLH}	Transition time, low- to high-level output†	See Figure 1			55	100	ns
t_{THL}	Transition time, high- to low-level output†				45	75	ns
t_{TLH}	Transition time, low- to high-level output‡	$R_L = 3$ kΩ to 7 kΩ,	$C_L = 2500$ pF,		2.5		µs
t_{THL}	Transition time, high- to low-level output‡	See Figure 1			3.0		µs

† Measured between 10% and 90% points of output waveform
‡ Measured between 3 V and – 3 V points on the output waveform (TIA/EIA-232-E conditions)

PARAMETER MEASUREMENT INFORMATION
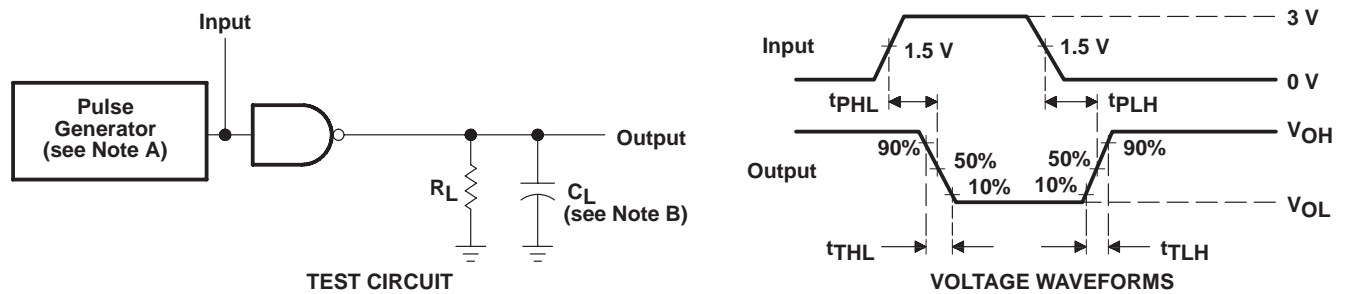
NOTES: A. The pulse generator has the following characteristics: $t_W = 0.5$ µs, PRR ≤ 1 MHz, $Z_O = 50$ Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

Figure 2

OUPUT CURRENT
vs
OUTPUT VOLTAGE

Figure 3

SHORT-CIRCUT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 4

SLEW RATE
vs
LOAD CAPACITANCE
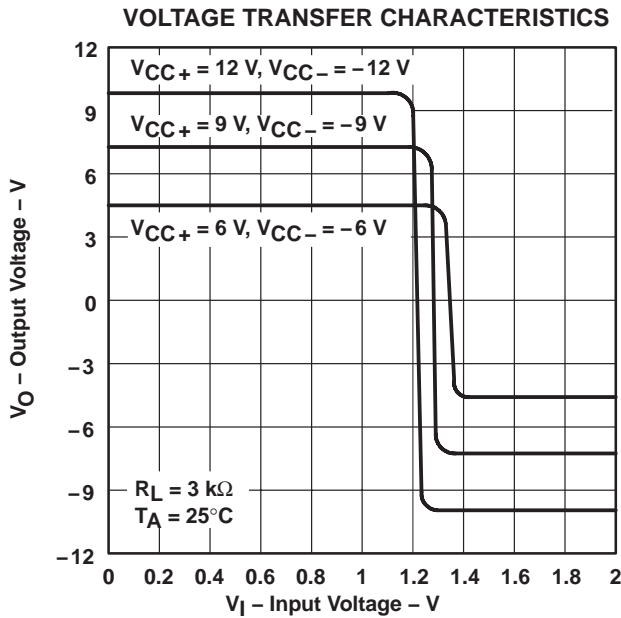
Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

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THERMAL INFORMATION†

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE
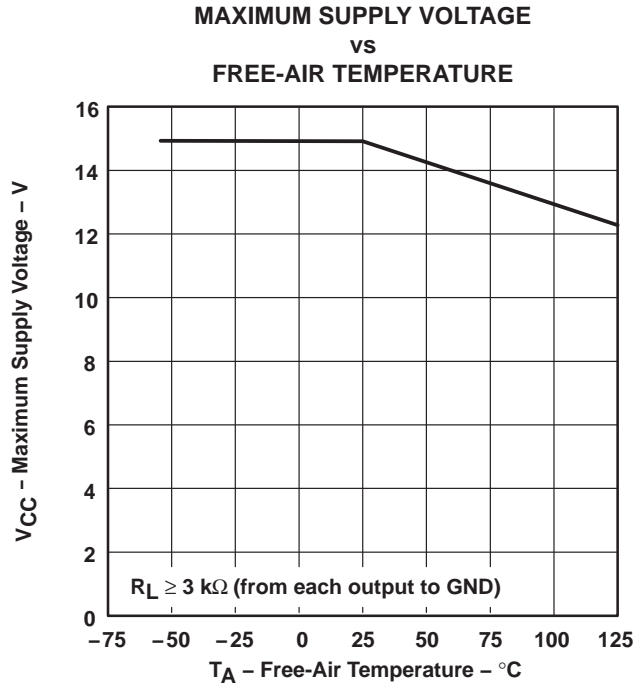
Figure 6

† Data for temperatures below 0°C and above 70°C are applicable to the SN55188 circuit only.

APPLICATION INFORMATION

Figure 7. Logic Translator Applications

Diodes placed in series with the V_{CC+} and V_{CC-} leads protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to ±15 V, and the power supplies are at low voltage and provide low-impedance paths to ground.

Figure 8. Power-Supply Protection to Meet Power-Off Fault Conditions of ANSI TIA/EIA-232-E

TEXAS
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PACKAGING INFORMATION

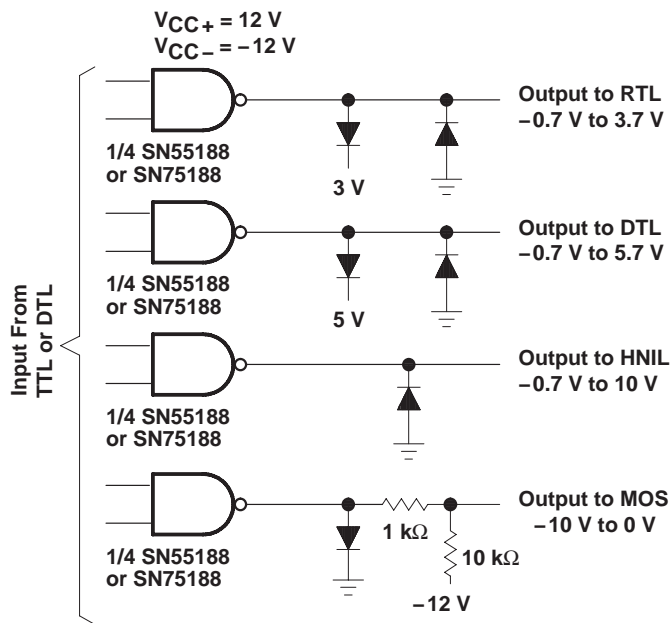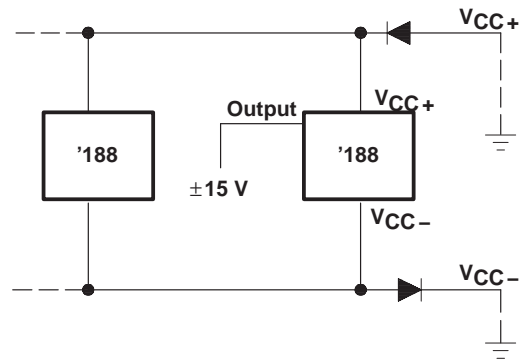| Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86889012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86889012A SNJ55 188FK	Samples
5962-8688901CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J	Samples
5962-8688901DA	ACTIVE	CFP	W	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W	Samples
MC1488N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1488N	Samples
MC1488NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1488N	Samples
SN55188J	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	SN55188J	Samples
SN75188D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	Samples
SN75188DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	Samples
SN75188DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	Samples
SN75188DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	Samples
SN75188N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75188N	Samples
SN75188NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	Samples
SNJ55188FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86889012A SNJ55 188FK	Samples
SNJ55188J	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J	Samples
SNJ55188W	ACTIVE	CFP	W	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55188, SN75188 :

● Catalog: SN75188

● Military: SN55188

NOTE: Qualified Version Definitions:

   ● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75188NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75188DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75188NSR	SO	NS	14	2000	367.0	367.0	38.0

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020 \ (0,51)}{0.010 \ (0,25)}$

$\frac{0.020 \ (0,51)}{0.010 \ (0,25)}$

$\frac{0.080 \ (2,03)}{0.064 \ (1,63)}$

$\frac{0.055 \ (1,40)}{0.045 \ (1,14)}$

$\frac{0.045 \ (1,14)}{0.035 \ (0,89)}$

$\frac{0.028 \ (0,71)}{0.022 \ (0,54)}$ 0.050 (1,27) $\frac{0.045 \ (1,14)}{0.035 \ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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MECHANICAL DATA

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.260 (6,60)
0.235 (5,97)

0.080 (2,03)
0.045 (1,14)

0.008 (0,20)
0.004 (0,10)

0.280 (7,11) MAX

1   14

0.019 (0,48)
0.015 (0,38)

0.050 (1,27)

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−2/F   04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL STD 1835 GDFP1−F14

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

TEXAS
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PIN 1 ID
(OPTIONAL)

A

1

14

12X .100
[2.54]

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015   GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

SEE DETAIL A

SEE DETAIL B

(.300) TYP
[7.62]

1

14

12X (.100)
[2.54]

SYMM
₵

14X (⌀ .039)
[1]

7

8

SYMM
₵

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(⌀ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
△C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   △D

Pin 1
Index Area

1   7

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
        △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
        △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←12x1,27

5,40

Stencil Openings
(Note D)

←14x0,55

14x1,50

←12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

─0,60

1,55

Example
Solder Mask Opening
(See Note E)

─0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      ⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      ⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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