

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	-60	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.14
Q_g max. (nC)	34	
Q_{gs} (nC)	9.9	
Q_{gd} (nC)	16	
Configuration	Single	

FEATURES

- Advanced process technology
- Surface mount (IRF9Z34S, SiHF9Z34S)
- 175 °C operating temperature
- Fast switching
- P-channel
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

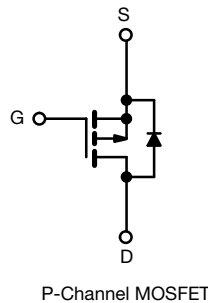
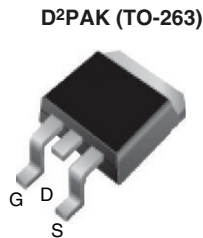
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.



ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9Z34S-GE3	SiHF9Z34STRL-GE3 ^a	SiHF9Z34STRR-GE3 ^a
Lead (Pb)-free	IRF9Z34SPbF	IRF9Z34STRLPbF ^a	IRF9Z34STRRPbF ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at -10 V	$T_C = 25$ °C	-18
		$T_C = 100$ °C	-13
Pulsed Drain Current ^{a, e}		I_{DM}	-72
Linear Derating Factor			0.59
Single Pulse Avalanche Energy ^{b, e}		E_{AS}	370
Avalanche Current ^a		I_{AR}	-18
Repetitive Avalanche Energy ^a		E_{AR}	8.8
Maximum Power Dissipation		$T_C = 25$ °C	88
		$T_A = 25$ °C	3.7
Peak Diode Recovery dV/dt ^{c, e}		dV/dt	-4.5
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175
Soldering Recommendations (Peak temperature) ^d		for 10 s	300

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25$ V, starting $T_J = 25$ °C, $L = 1.3$ mH, $R_g = 25$ Ω , $I_{AS} = -18$ A (see fig. 12).
- $I_{SD} \leq -18$ A, $dI/dt \leq 170$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.
- Uses IRF9Z34, SiHF9Z34 data and test conditions.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7	

Note

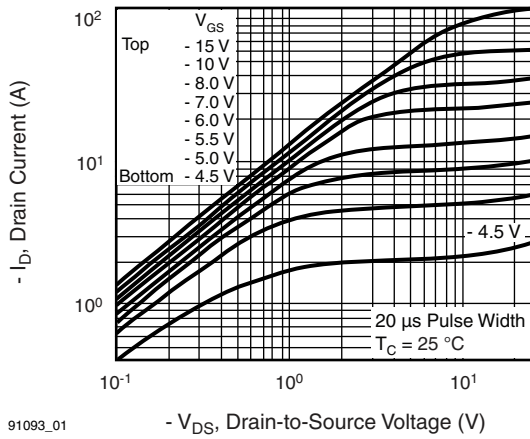
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA ^c	-	-0.06	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	-	-	-100	μA
		V _{DS} = -48 V, V _{GS} = 0 V, T _J = 150 °C	-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -11 A ^b	-	-	0.14	Ω
Forward Transconductance	g _{fs}	V _{DS} = -25 V, I _D = -11 A ^c	5.9	-	-	S
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5 ^c	-	1100	-	pF
Output Capacitance	C _{oss}		-	620	-	
Reverse Transfer Capacitance	C _{rss}		-	100	-	
Total Gate Charge	Q _g	V _{GS} = -10 V, I _D = -18 A, V _{DS} = -48 V, see fig. 6 and 13 ^{b, c}	-	-	34	nC
Gate-Source Charge	Q _{gs}		-	-	9.9	
Gate-Drain Charge	Q _{gd}		-	-	16	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, I _D = -18 A, R _g = 12 Ω, R _D = 1.5 Ω, see fig. 10 ^{b, c}	-	18	-	ns
Rise Time	t _r		-	120	-	
Turn-Off Delay Time	t _{d(off)}		-	20	-	
Fall Time	t _f		-	58	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain	0.7	-	3.9	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	-18	A
Pulsed Diode Forward Current ^a	I _{SM}		-	-	-72	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -18 A, V _{GS} = 0 V ^b	-	-	-6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -18 A, di/dt = 100 A/μs ^{b, c}	-	100	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	280	520	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

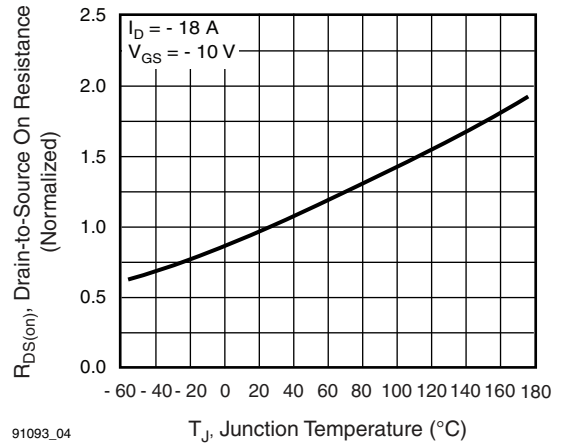
- b. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- c. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- d. Uses IRF9Z34, SiHF9Z34 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



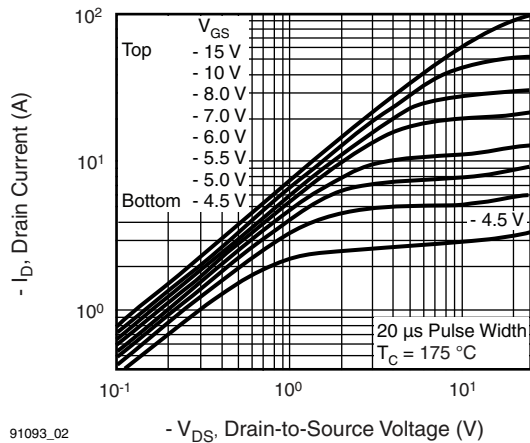
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Fig. 1 - Typical Output Characteristics



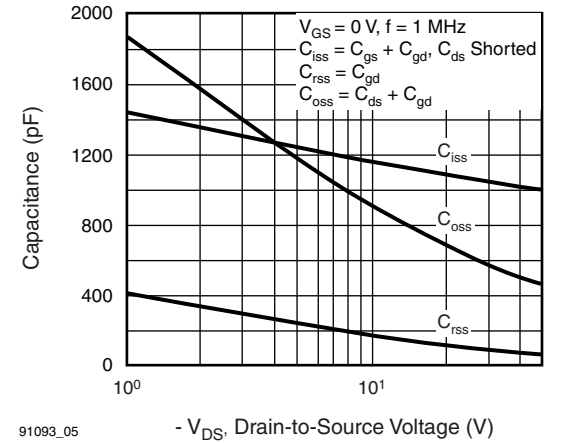
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Fig. 4 - Normalized On-Resistance vs. Temperature



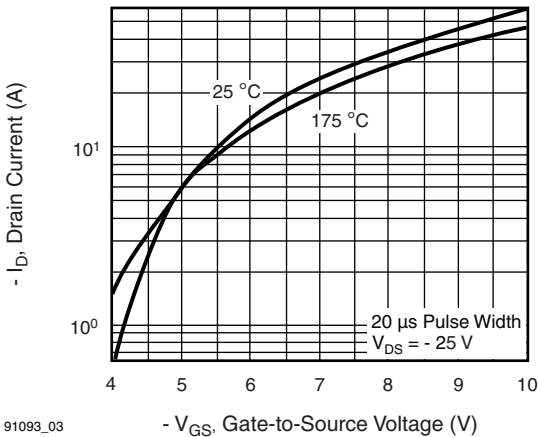
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Fig. 2 - Typical Output Characteristics



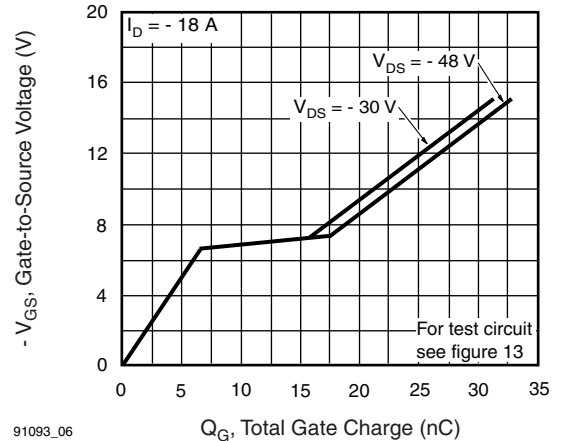
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



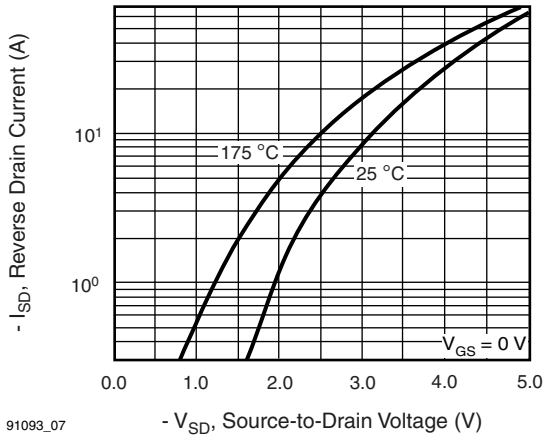
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Fig. 3 - Typical Transfer Characteristics



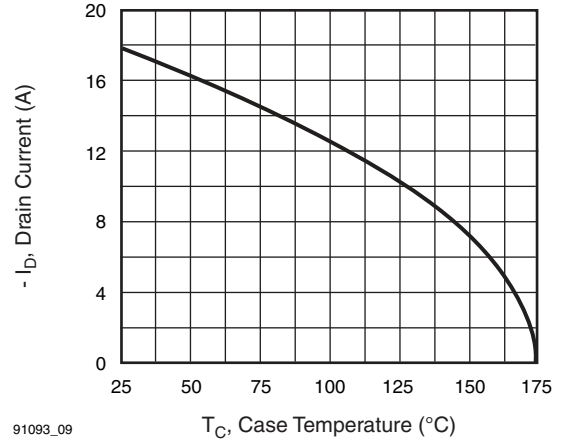
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



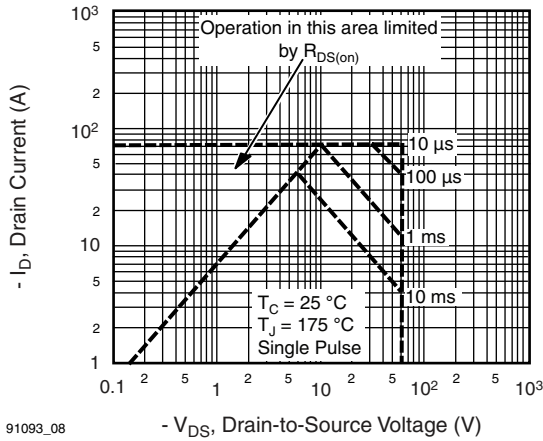
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

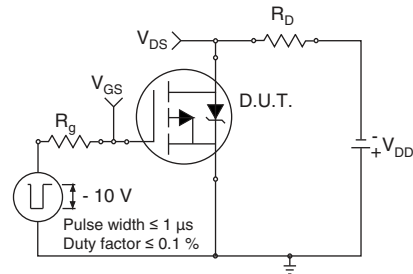


Fig. 10a - Switching Time Test Circuit

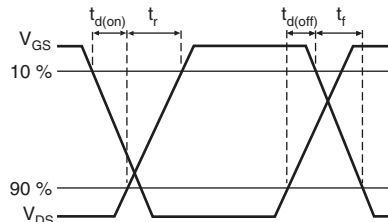
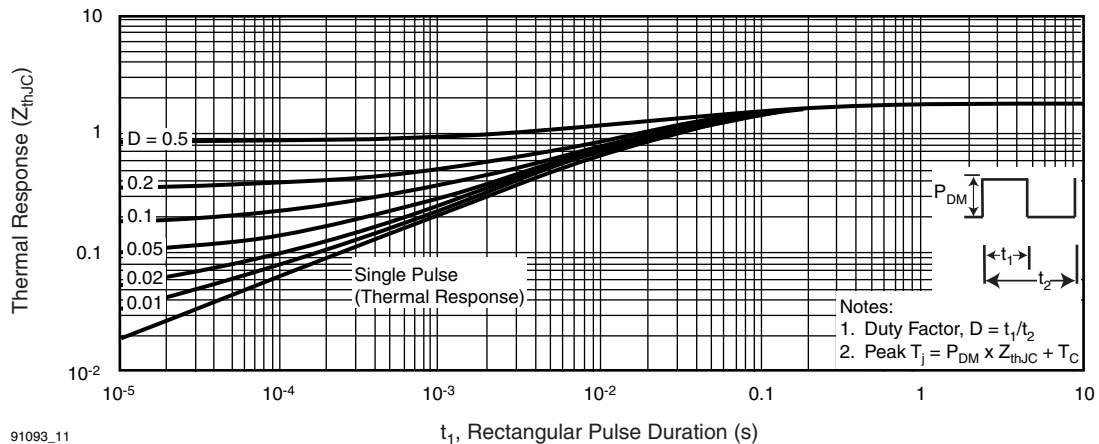


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

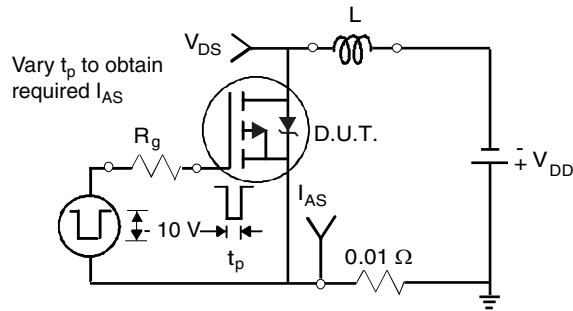


Fig. 12a - Unclamped Inductive Test Circuit

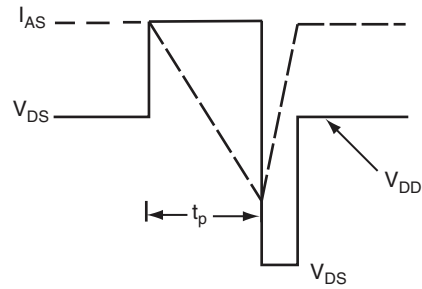


Fig. 12b - Unclamped Inductive Waveforms

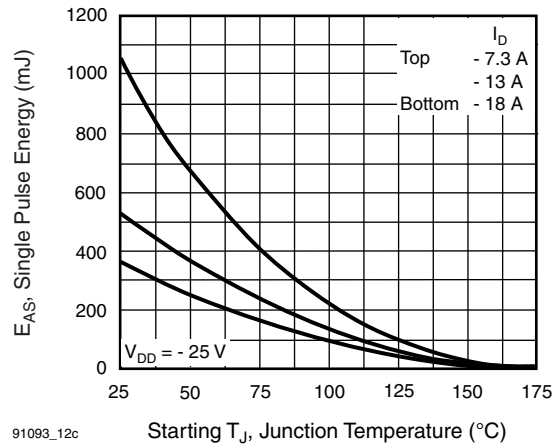


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

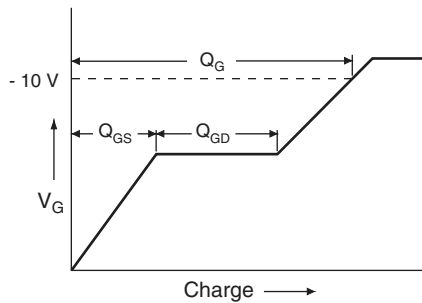


Fig. 13 - Maximum Avalanche Energy vs. Drain Current

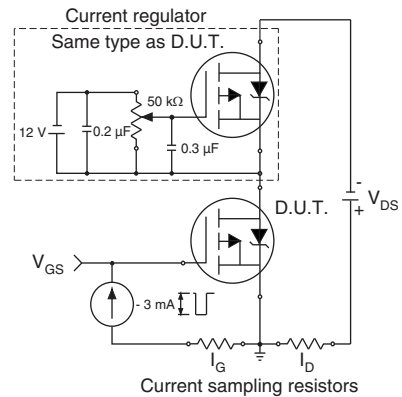
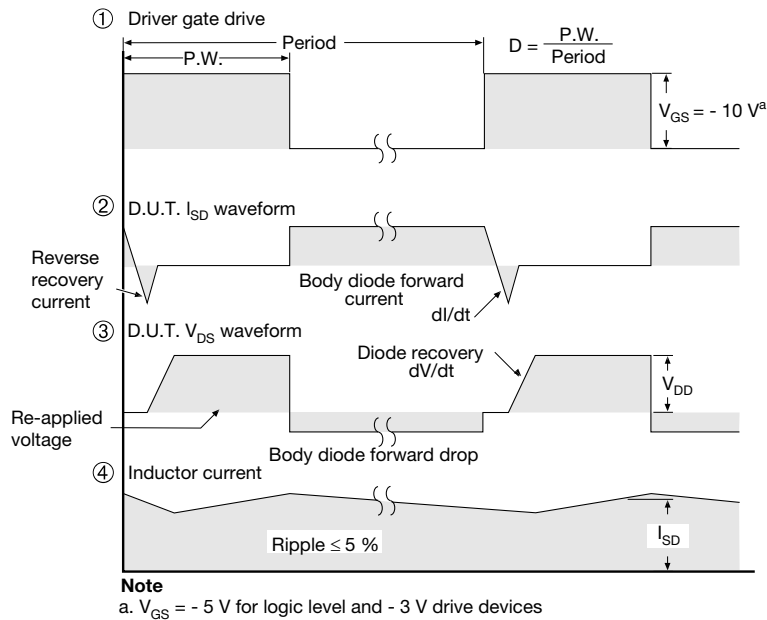
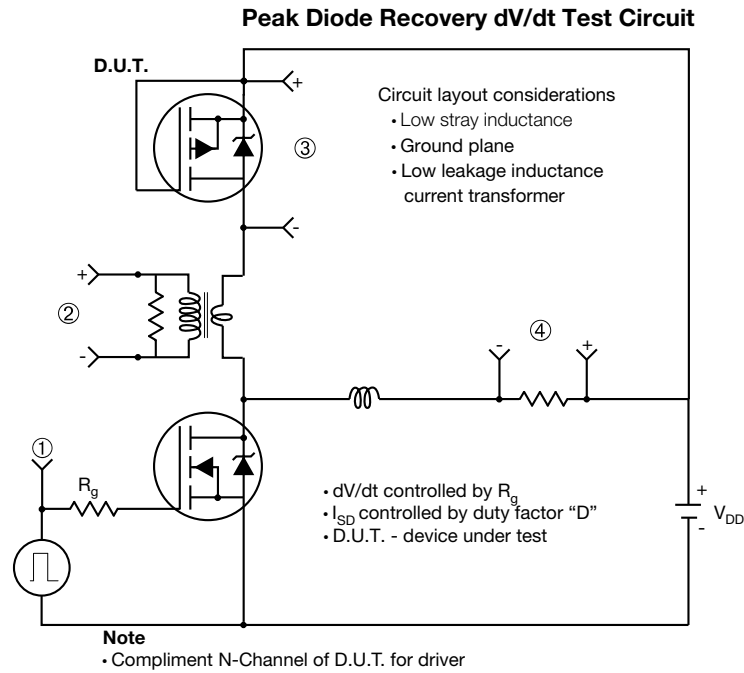


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For P-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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