HM-6504

4096 x 1 CMOS RAM

Features

- LOW POWER STANDBY — 125 μW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- EXTREMELY LOW SPEED-POWER PRODUCT
- DATA RETENTION — @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 120/200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- GATED INPUTS-NO PULL UP OR PULL DOWN RESISTORS REQUIRED

Description

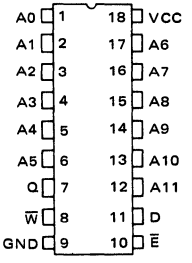
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

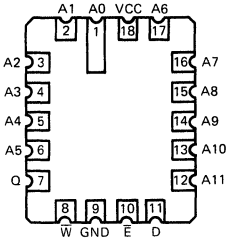
Data retention supply voltage and supply current are guaranteed over temperature.

Pinouts

TOP VIEW

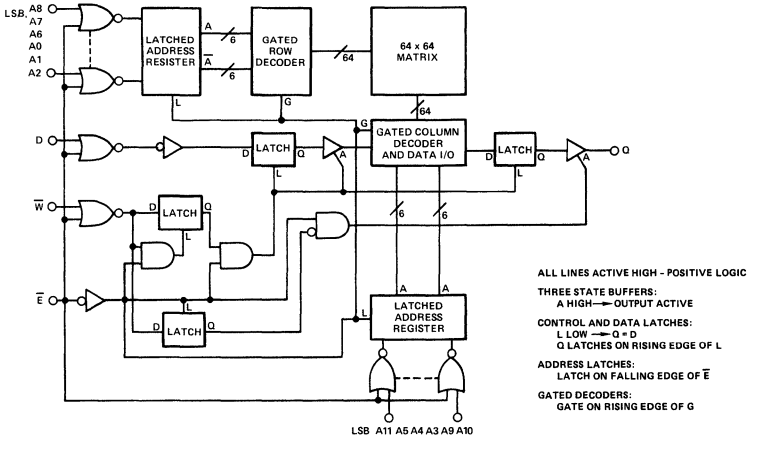


TOP VIEW



A — Address Input
$\overline{E}$ — Chip Enable
$\overline{W}$ — Write Enable
D — Data Input
Q — Data Output

Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	μA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	μA	IO = 0, VCC = 2.0V $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	20			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	40			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	25			ns	(4)
	TELDX	Early Write Data Hold Time	25			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Industrial (-9)	-40°C to +85°C

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ELECTRICAL CHARACTERISTICS PRELIMINARY

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	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	20			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	40			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	25			ns	(4)
	TELDX	Early Write Data Hold Time	25			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information,– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	µA	VCC = 2.0 V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200		ns	(4)
	TAVQV	Address Access Time		220		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	200			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	60			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	150			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	60			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	60			ns	(4)
	TELDX	Early Write Data Hold Time	60			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	290			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10ns; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

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ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current ②		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200		ns	④
	TAVQV	Address Access Time		220		ns	④
	TELQX	Chip Enable Output Enable Time	20			ns	④
	TEHQZ	Chip Enable Output Disable Time		80		ns	④⑤
	TELEH	Chip Enable Pulse Negative Width	200			ns	④
	TEHEL	Chip Enable Pulse Positive Width	90			ns	④
	TAVEL	Address Setup Time	20			ns	④
	TELAX	Address Hold Time	50			ns	④
	TWLWH	Write Enable Pulse Width	60			ns	④
	TWLEH	Write Enable Pulse Setup Time	150			ns	④
	TWLEL	Early Write Pulse Setup Time	0			ns	④
	TWHEL	Write Enable Read Mode Setup Time	0			ns	④
	TELWH	Early Write Pulse Hold Time	60			ns	④
	TDVWL	Data Setup Time	0			ns	④
	TDVEL	Early Write Data Setup Time	0			ns	④
	TWLDX	Data Hold Time	60			ns	④
	TELDX	Early Write Data Hold Time	60			ns	④
	TQVWL	Data Valid to Write Time	0			ns	④
	TELEL	Read or Write Cycle Time	290			ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
⑤ This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

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D.C.	ICCSB	Standby Supply Current		50	5.0	μA	IO = 0 $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Industrial (-9)	-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

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	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
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	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4)(5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

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(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Industrial (-9)	-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	20	µA	IO = 0 $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		50	12	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4)(5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

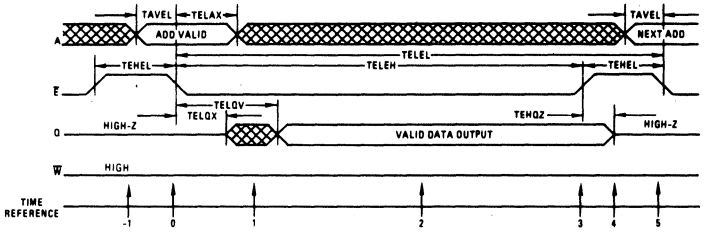
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		350	50	μA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		200	30	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		ns	(4)
	TAVQV	Address Access Time		370		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	350			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	100			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	250			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	100			ns	(4)
	TDVWL	Data Setup Time	30			ns	(4)
	TDVEL	Early Write Data Setup Time	30			ns	(4)
	TWLDX	Data Hold Time	100			ns	(4)
	TELDX	Early Write Data Hold Time	100			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	500			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

Read Cycle

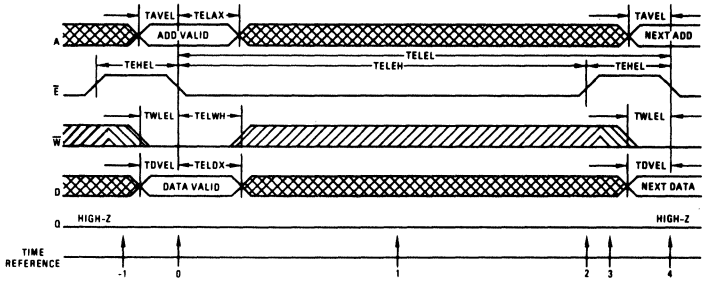


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

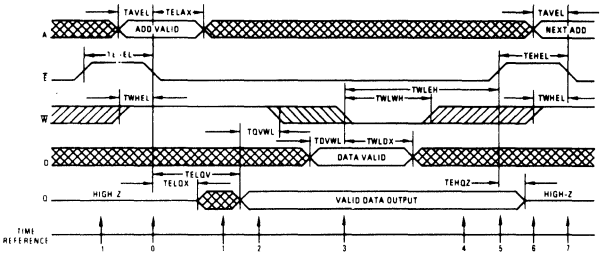


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

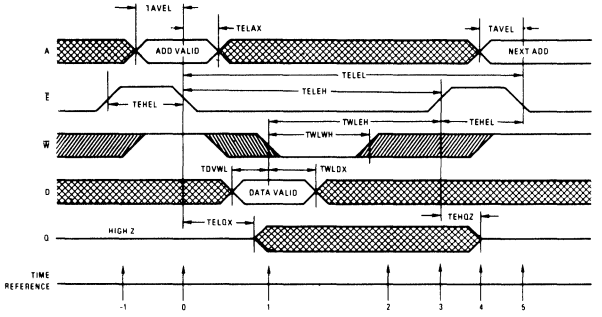


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↘	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↗	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches and disables all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↘	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↗	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.