May 2014

FDMS7620S

Dual N-Channel PowerTrench® MOSFET
Q1: 30 V, 13 A, 20.0 mΩ Q2: 30 V, 22 A, 11.2 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 20.0 mΩ at V_{GS} = 10 V, I_D = 10.1 A
- Max $r_{DS(on)}$ = 30.0 mΩ at V_{GS} = 4.5 V, I_D = 7.5 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 11.2 mΩ at V_{GS} = 10 V, I_D = 12.4 A
- Max $r_{DS(on)}$ = 14.2 mΩ at V_{GS} = 4.5 V, I_D = 10.9 A
- Pinout optimized for simple PCB design
- Thermally efficient dual Power 56 Package
- RoHS Compliant

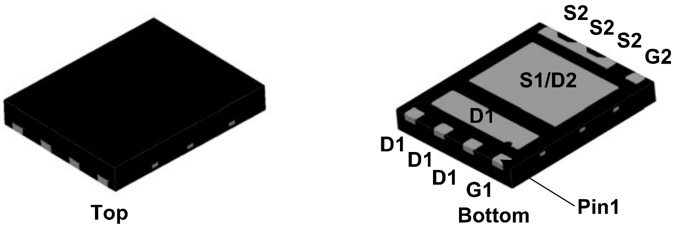
General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal synchronous buck power stage in terms of efficiency and PCB utilization. The low switching loss “High Side” MOSFET is complementory by a low conduction loss “Low Side” SyncFET.

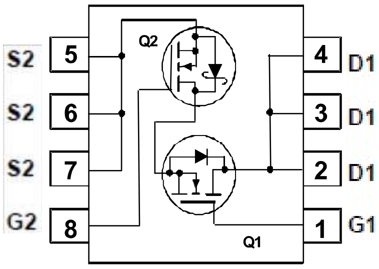
Applications

Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load



Power 56



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	13	22	A
	-Continuous	T_A = 25 °C	10.1	12.4	
	-Pulsed		27	45	
E_{AS}	Single Pulse Avalanche Energy	(Note 4)	9	21	mJ
P_D	Power Dissipation for Single Operation	T_A = 25°C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25°C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7620S	FDMS7620S	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		19 19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	µA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	Q1 Q2			100 100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 µA $V_{GS} = V_{DS}$, I_D = 1 mA	Q1 Q2	1.0 1.0	2.2 2.0	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		-6 -5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10.1 A V_{GS} = 4.5 V, I_D = 7.5 A V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	Q1		15.2 22.7 18.7	20.0 30.0 22.5	mΩ
		V_{GS} = 10 V, I_D = 12.4 A V_{GS} = 4.5 V, I_D = 10.9 A V_{GS} = 10 V, I_D = 12.4 A, T_J = 125°C	Q2		8.3 10.5 8.9	11.2 14.2 15.1	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 10.1 A V_{DD} = 5 V, I_D = 12.4 A	Q1 Q2		22 53		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		457 1050	608 1400	pF
C_{oss}	Output Capacitance		Q1 Q2		167 358	222 477	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		22 35	31 49	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 1.2	4.4 3.5	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 10.1 A, R_{GEN} = 6 Ω Q2 V_{DD} = 15 V, I_D = 12.4 A, R_{GEN} = 6 Ω		Q1 Q2		5.2 6.6	10 14	ns
t_r	Rise Time			Q1 Q2		1.2 1.8	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time			Q1 Q2		11.9 17.4	22 32	ns
t_f	Fall Time			Q1 Q2		1.4 1.5	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 10 V	Q1 V_{DD} = 15 V, I_D = 10.1 A Q2 V_{DD} = 15 V, I_D = 12.4 A	Q1 Q2		7.2 15.6	11 23	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 5 V		Q1 Q2		3.8 7.9	6 12	nC
Q_{gs}	Gate to Source Charge			Q1 Q2		1.6 3.2		nC
Q_{gd}	Gate to Drain “Miller” Charge			Q1 Q2		1.1 1.6		nC

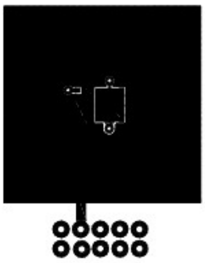
Electrical Characteristics T_J = 25°C unless otherwise noted

Drain-Source Diode Characteristics

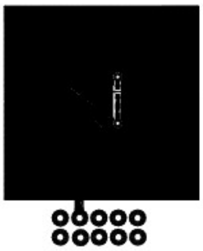
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 10.1 A (Note 2) V_{GS} = 0 V, I_S = 12.4 A (Note 2)	Q1 Q2		0.90 0.83	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 10.1 A, di/dt = 100 A/s Q2 I_F = 12.4 A, di/dt = 300 A/s	Q1 Q2		16 18	28 32	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2		4 13	10 23	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

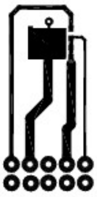


a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper

c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

4. Q1: E_{AS} of 9 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 8 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 12 A.

Q2: E_{AS} of 21 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 18 A.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

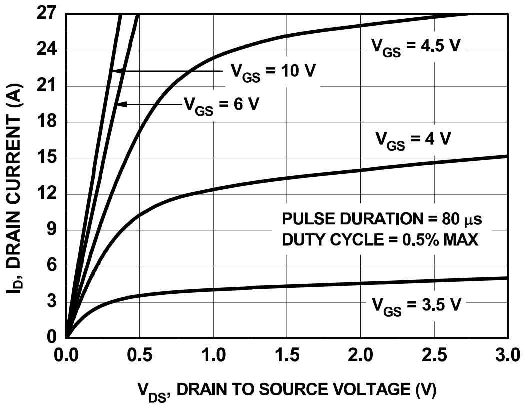


Figure 1. On Region Characteristics

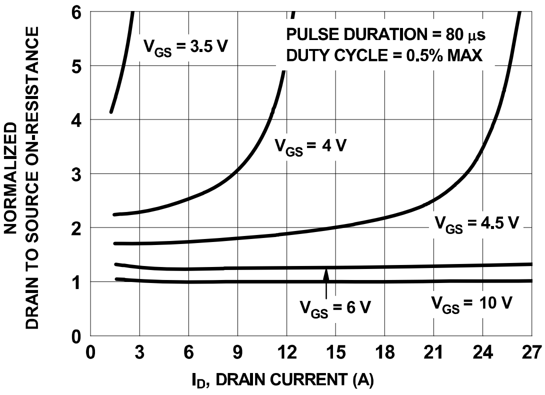


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

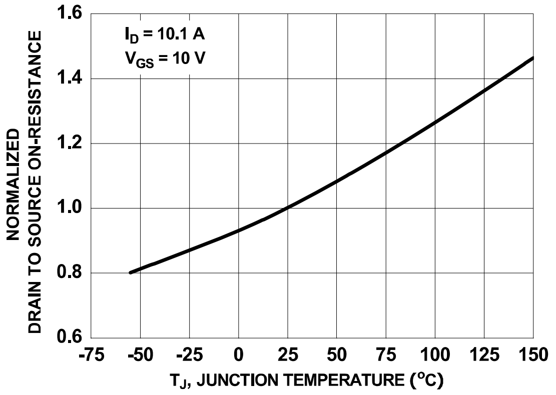


Figure 3. Normalized On Resistance vs Junction Temperature

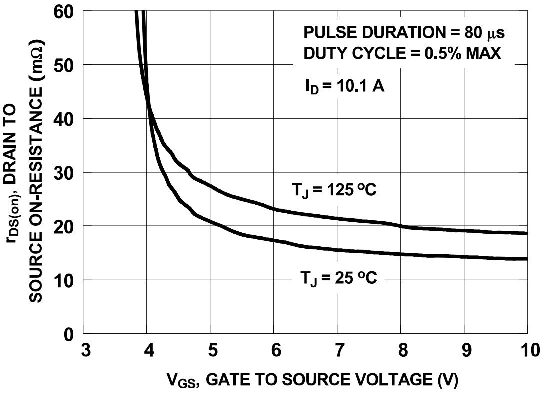


Figure 4. On-Resistance vs Gate to Source Voltage

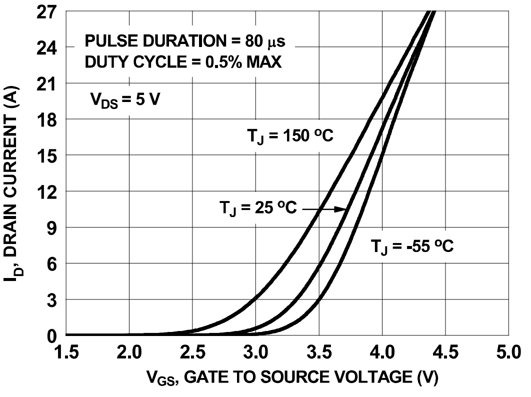


Figure 5. Transfer Characteristics

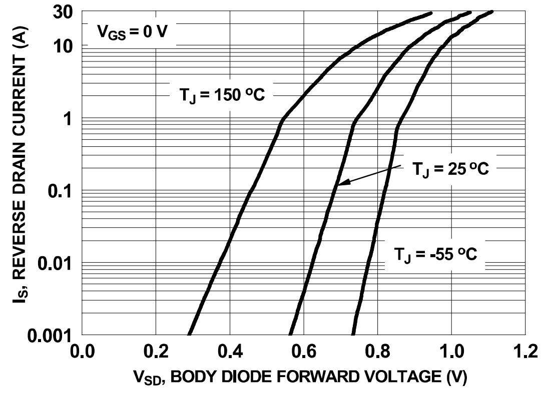


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

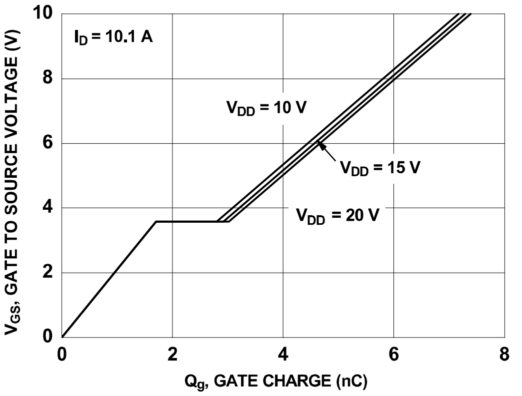


Figure 7. Gate Charge Characteristics

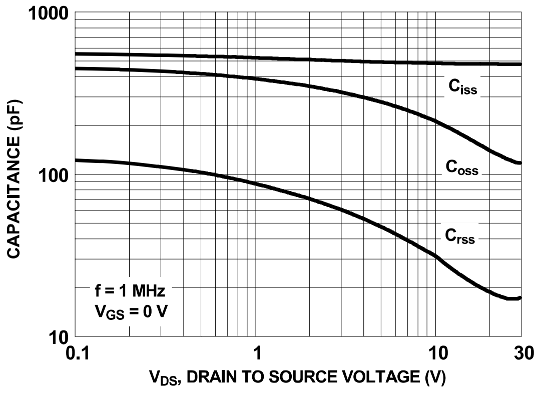


Figure 8. Capacitance vs Drain to Source Voltage

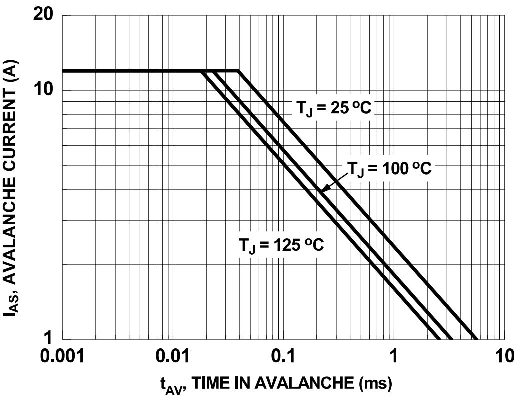


Figure 9. Unclamped Inductive Switching Capability

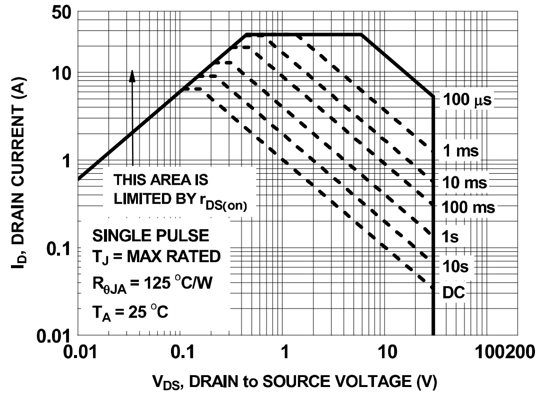


Figure 10. Forward Bias Safe Operating Area

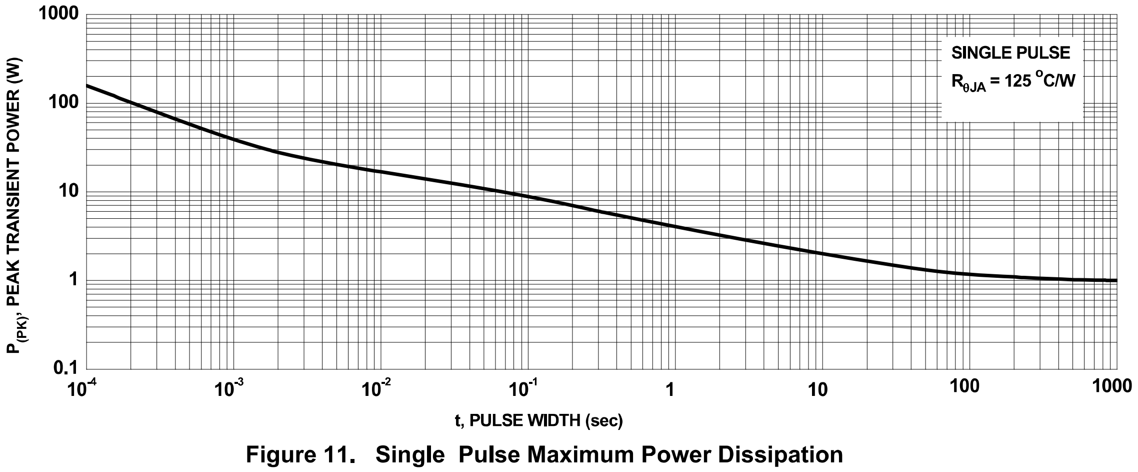


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

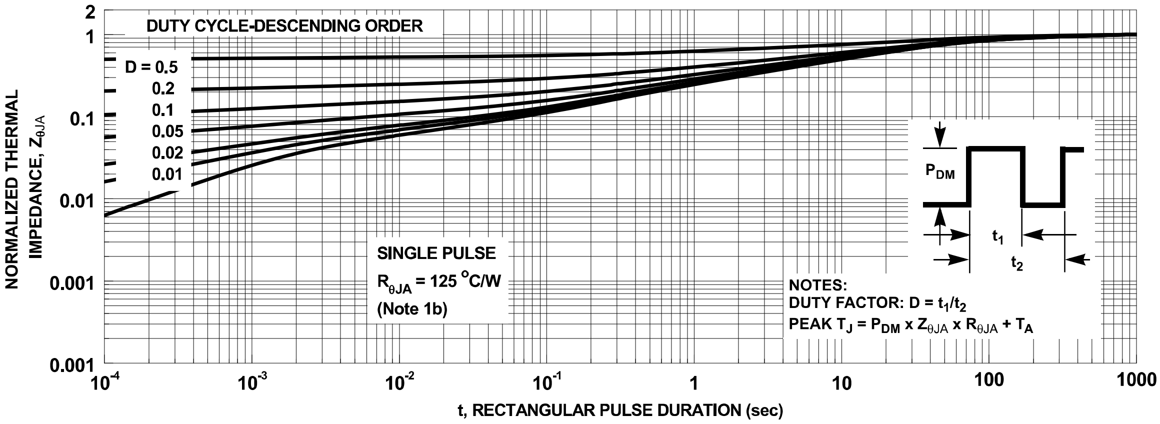


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

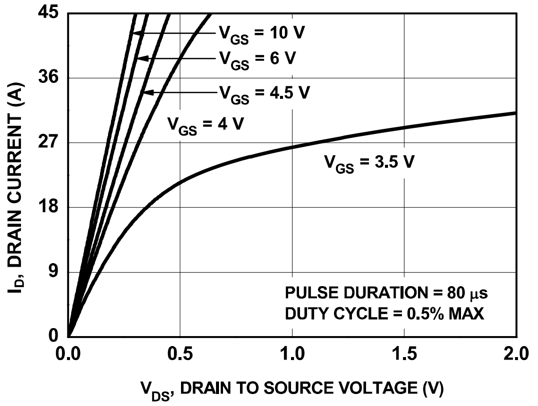


Figure 13. On-Region Characteristics

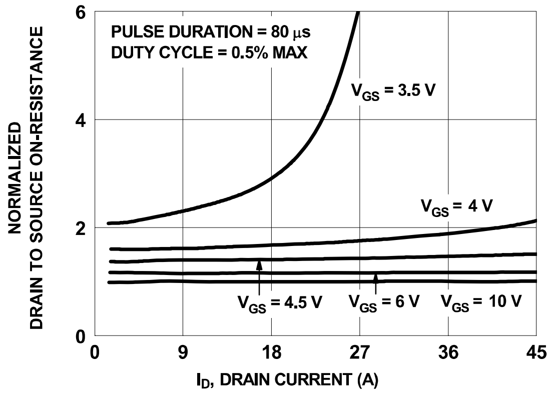


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

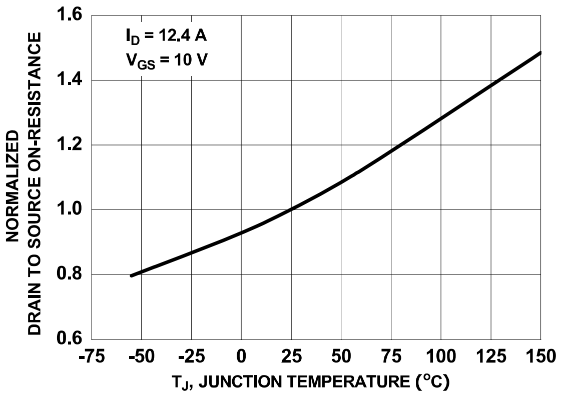


Figure 15. Normalized On-Resistance vs Junction Temperature

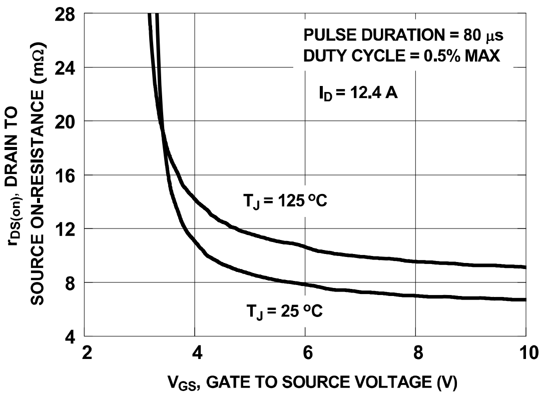


Figure 16. On-Resistance vs Gate to Source Voltage

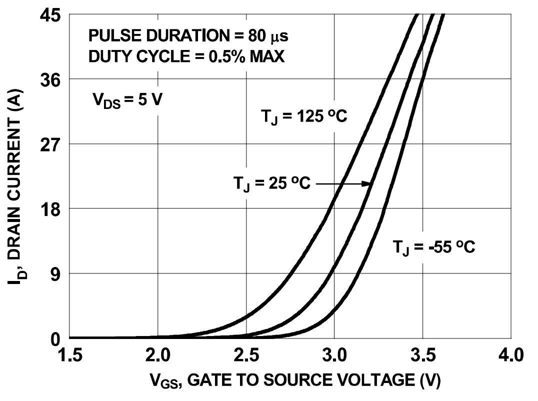


Figure 17. Transfer Characteristics

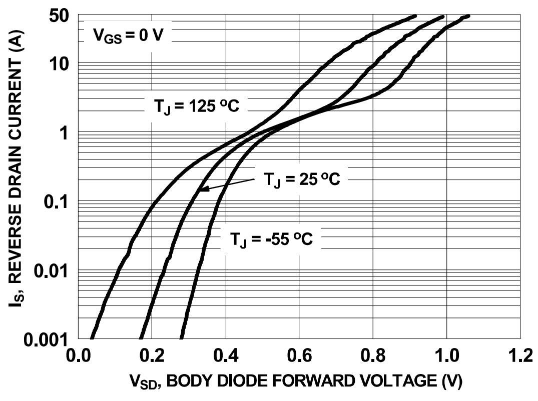


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

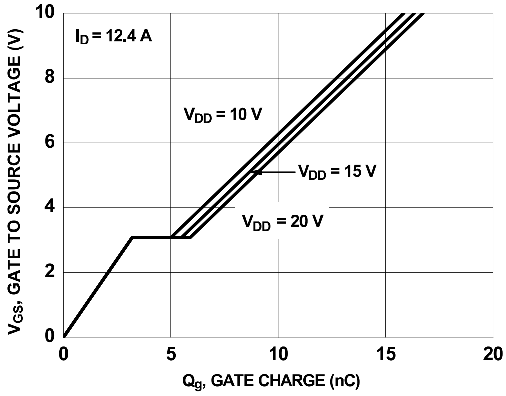


Figure 19. Gate Charge Characteristics

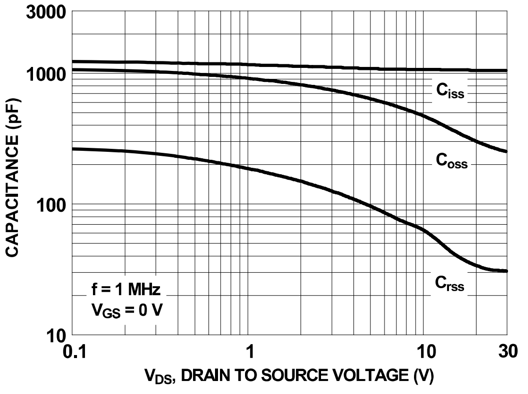


Figure 20. Capacitance vs Drain to Source Voltage

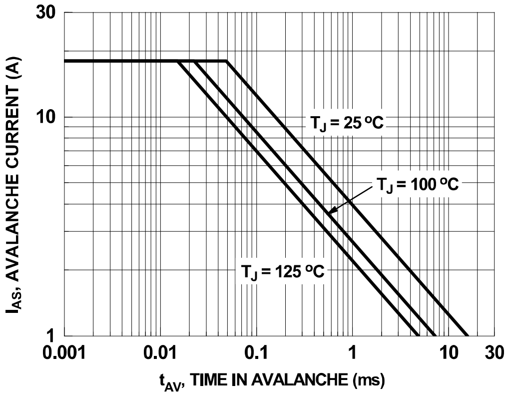


Figure 21. Unclamped Inductive Switching Capability

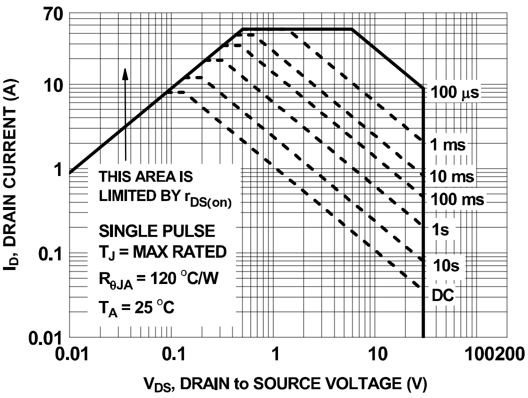


Figure 22. Forward Bias Safe Operating Area

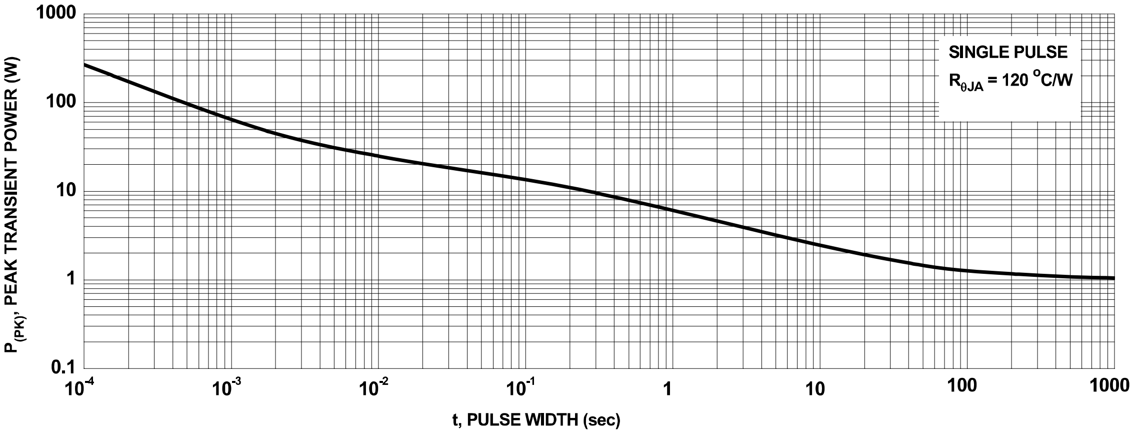


Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

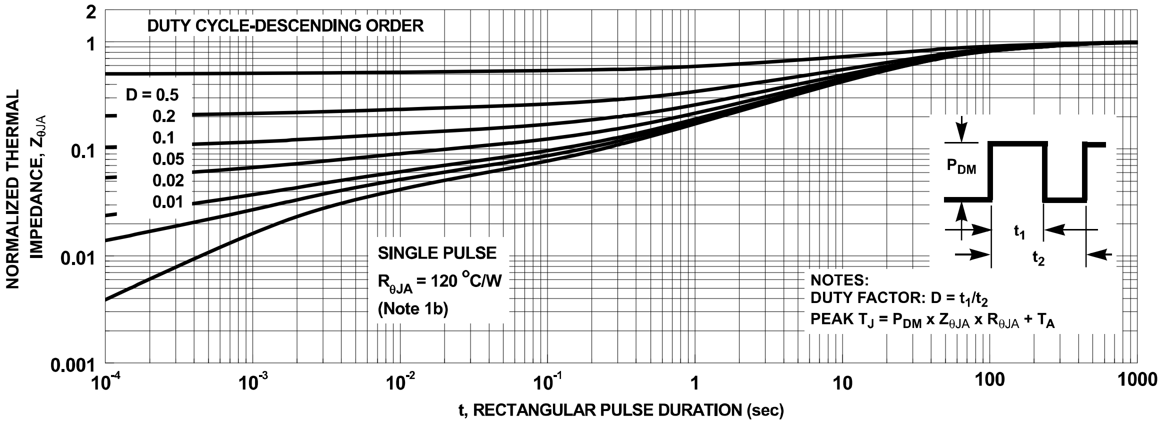


Figure 24. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET^{TM} Schottky body diode Characteristics

Fairchild's SyncFET^{TM} process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 26 shows the reverse recovery characteristic of the FDMS7620S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

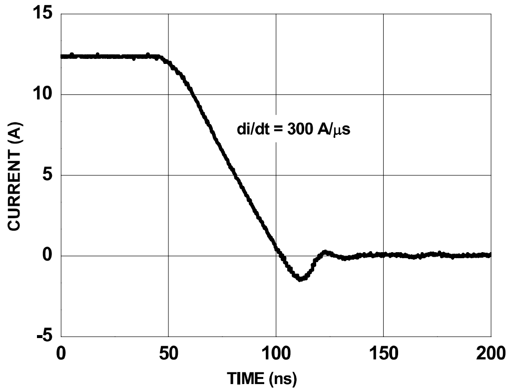


Figure 25. FDMS7620S SyncFET^{TM} Body Diode Reverse Recovery Characteristic

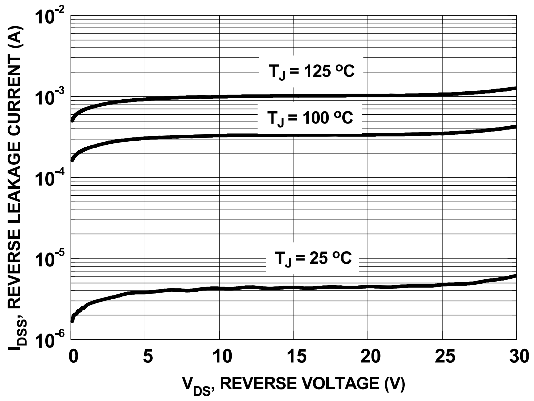
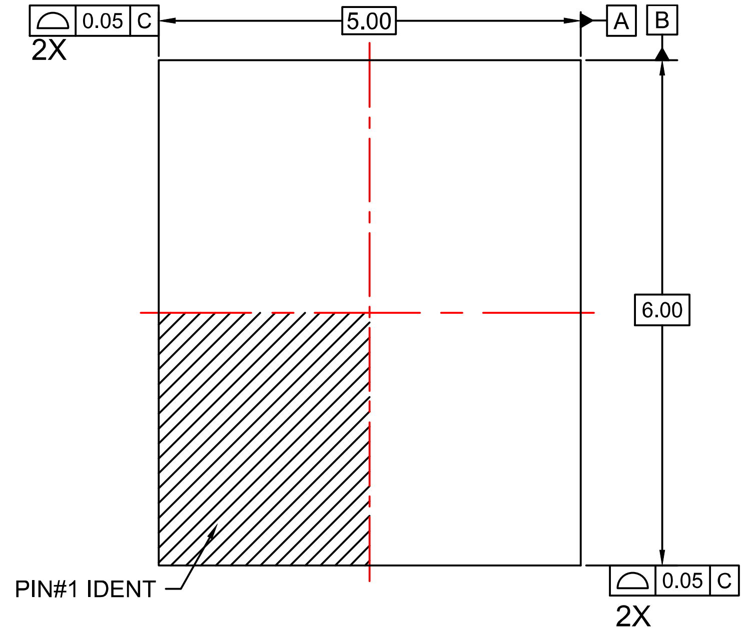
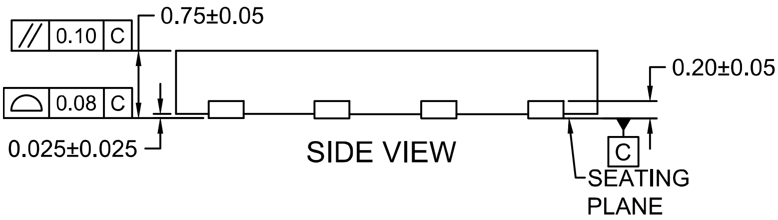
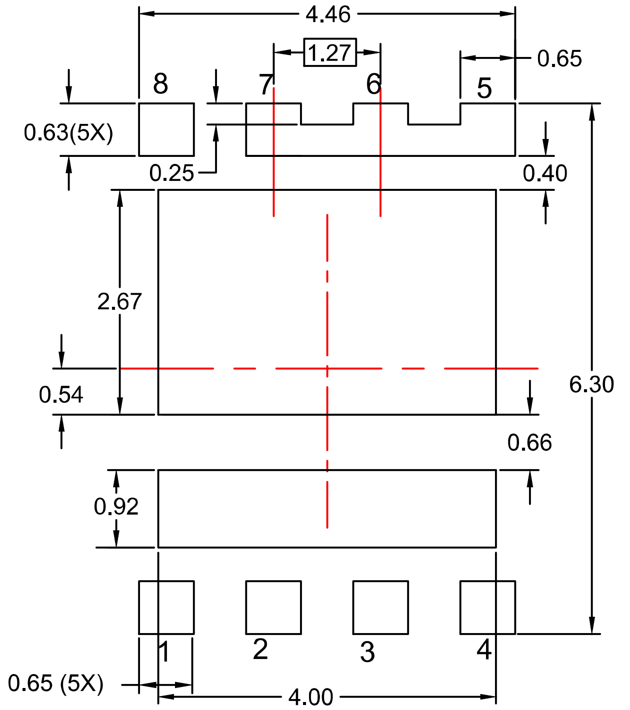


Figure 26. SyncFET^{TM} Body Diode Reverse Leakage vs. Drain-Source Voltage

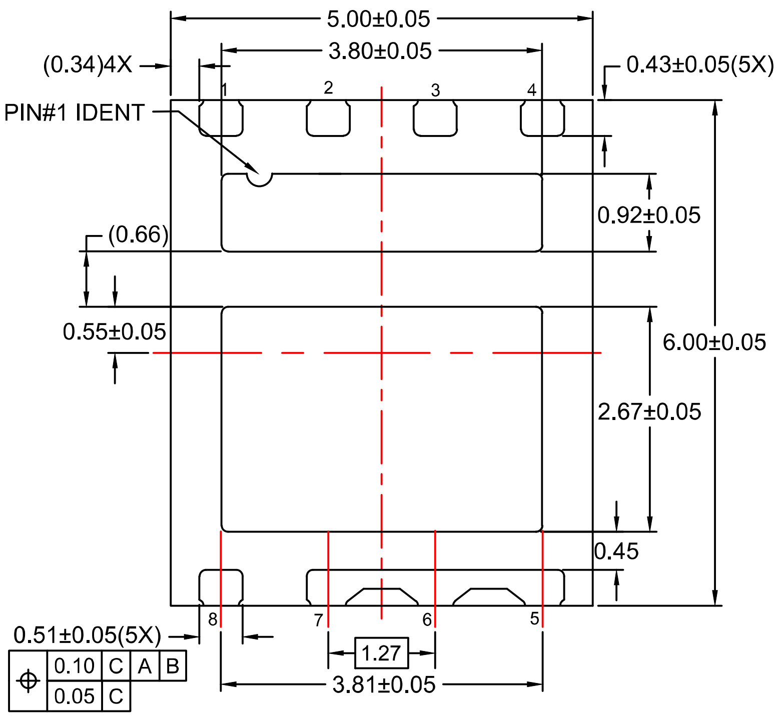




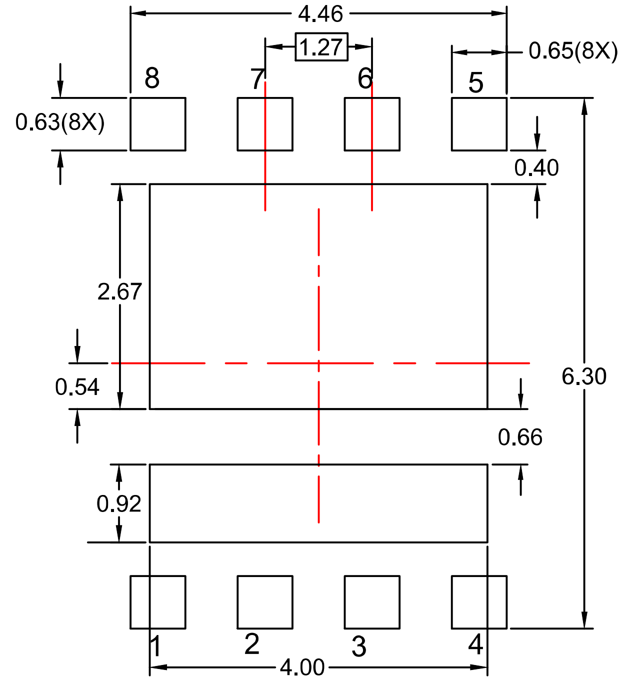
SIDE VIEW



RECOMMENDED LAND PATTERN
(OPTION 1 - FUSED LEADS 5,6,7)



BOTTOM VIEW



RECOMMENDED LAND PATTERN
(OPTION 2 - ISOLATED LEADS)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Prev2.

FAIRCHILD.