National Semiconductor

DS34C86T
Quad CMOS Differential Line Receiver

General Description

The DS34C86T is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86T has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

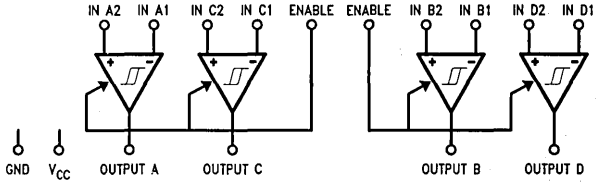
The DS34C86T features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86T is pin compatible with the DS3486.

Features

- CMOS design for low power
- ±0.2V sensitivity over the input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for system bus compatibility
- Available in surface mount
- Open input Failsafe feature, output high for open input

Logic Diagram



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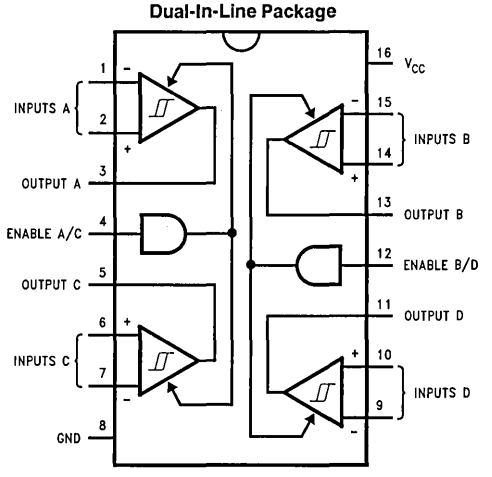
Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS34C86TJ, DS34C86TM, and DS34C86TN
See NS Package Number J16A, M16A and N16E

Truth Table

Enable	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	H
H	$V_{ID} \leq V_{TH}$ (Min)	L
H	Open*	H

*Open, not terminated
Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Package	2308 mW
Plastic "N" Package	1645 mW
SOIC Package	1190 mW
Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	5.0	6.8	10	kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		+1.1 −2.0	+1.5 −2.5	mA mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)} = -1V$ I_{OUT} = 6.0 mA		0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)} = +1V$		16	23	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V		60		mV

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3) (*Figures 1, 2,* and *3*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		19	30	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	18	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	21	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the operating temperature range.

All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: ESD Rating; HBM (1.5kΩ, 100 pF)
Inputs ≥ 2000V
All other pins ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C and M Package 9.52 mW/°C.

Comparison Table of Switching Characteristics into "LS-Type" Load

V_{CC} = 5V, T_A = 25°C (*Figures 4* and *5*) (Note 6)

Symbol	Parameter	DS34C86		DS3486		Units
		Typ	Max	Typ	Max	
$t_{PHL(D)}$	Propagation Delay Time Output High to Low	17		19		ns
$t_{PLH(D)}$	Propagation Delay Time Output Low to High	19		19		ns
t_{PLZ}	Output Low to TRI-STATE	13		23		ns
t_{PHZ}	Output High to TRI-STATE	12		25		ns
t_{PZH}	Output TRI-STATE to High	13		18		ns
t_{PZL}	Output TRI-STATE to Low	13		20		ns

Note 6: This Table is provided for comparison purposes only. The values in this table for the DS34C86 reflect the performance of the device but are not tested or guaranteed.

Test and Switching Waveforms

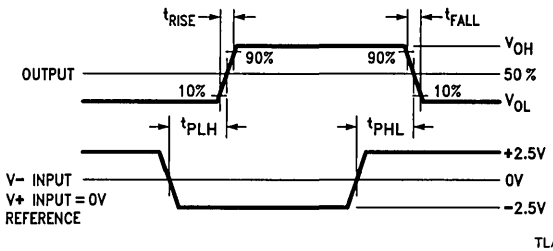

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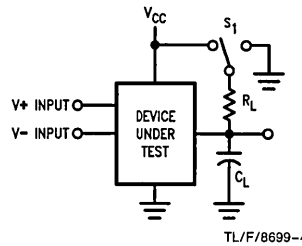
FIGURE 1. Propagation Delays



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C_L Includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

Test and Switching Waveforms (Continued)

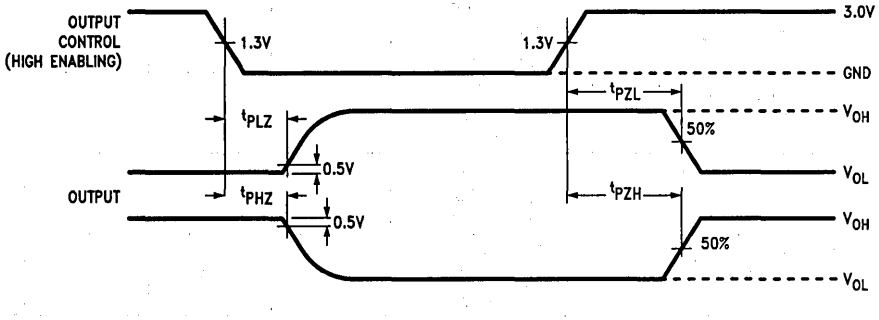
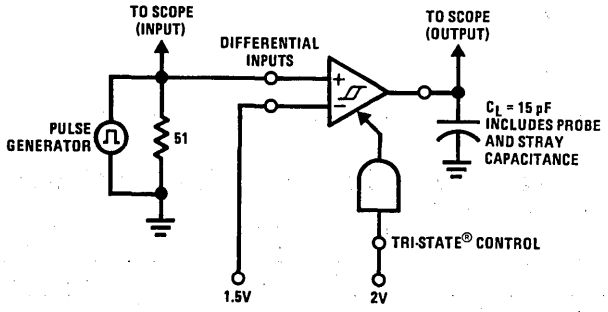
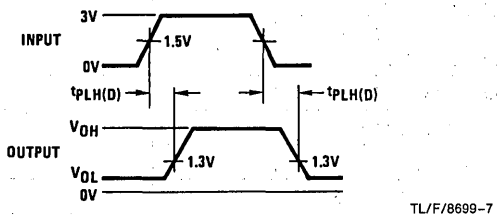


FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuits and Switching Time Waveforms

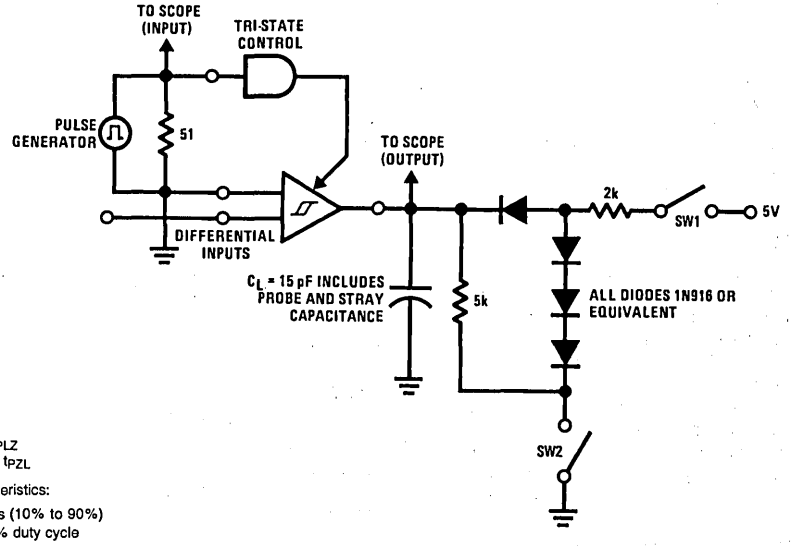




Input Pulse Characteristics:
$t_{TLH} = t_{THL} = 6$ ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 4. Propagation Delay Differential Input to Output for "LS-Type" Load

AC Test Circuits and Switching Time Waveforms (Continued)



1.5V for t_{PHZ} and t_{PLZ}
−1.5V for t_{PLZ} and t_{PZL}

Input Pulse Characteristics:

$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

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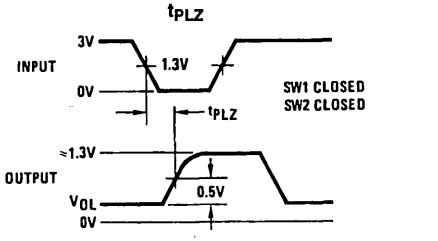

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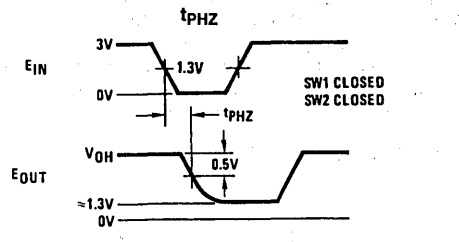

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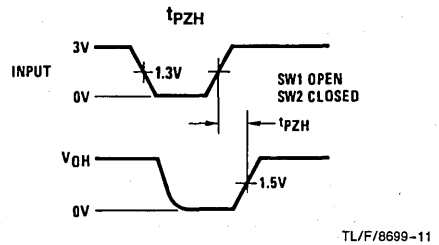

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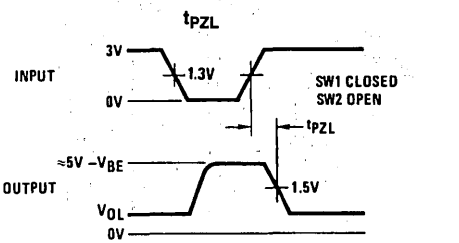

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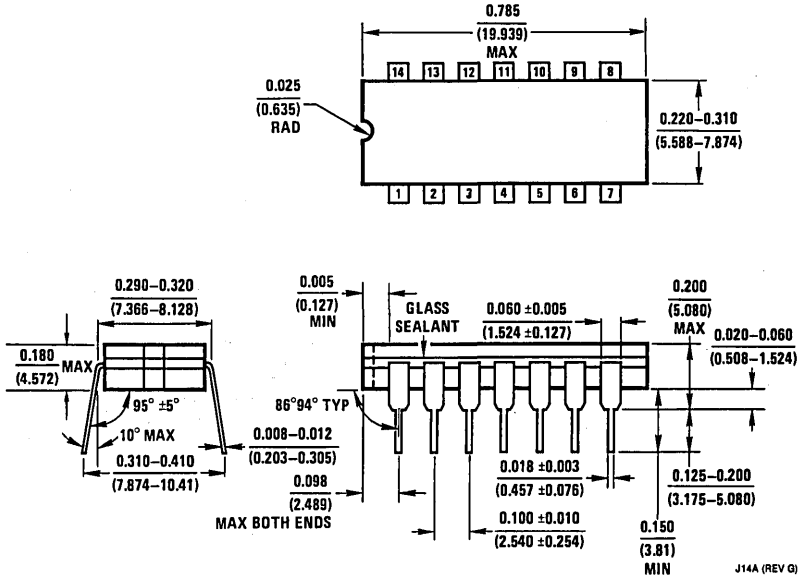
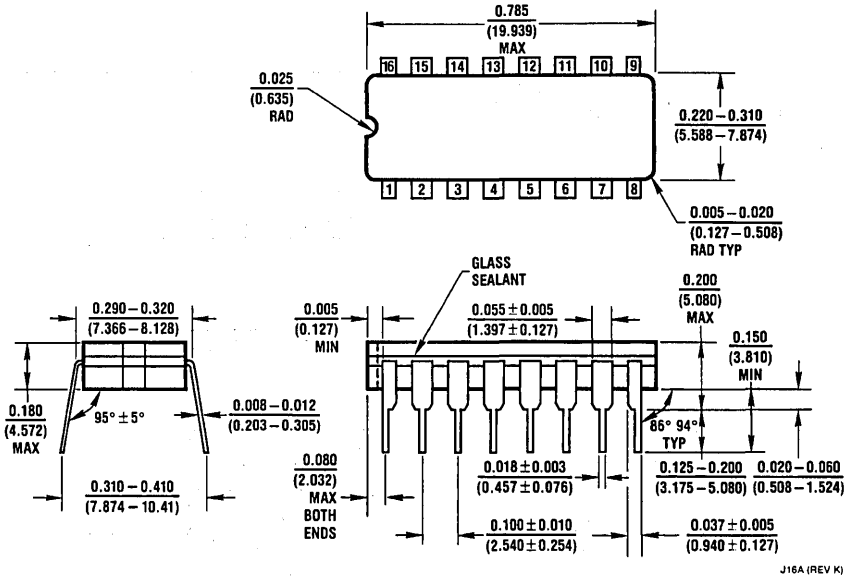
FIGURE 5. Propagation Delay TRI-STATE Control Unit to Output for "LS-Type" Load

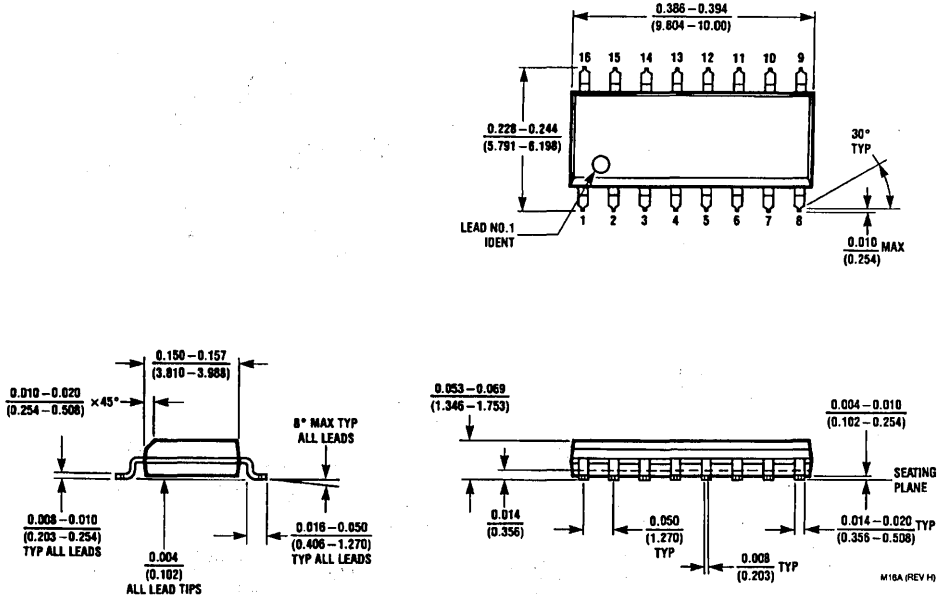
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A



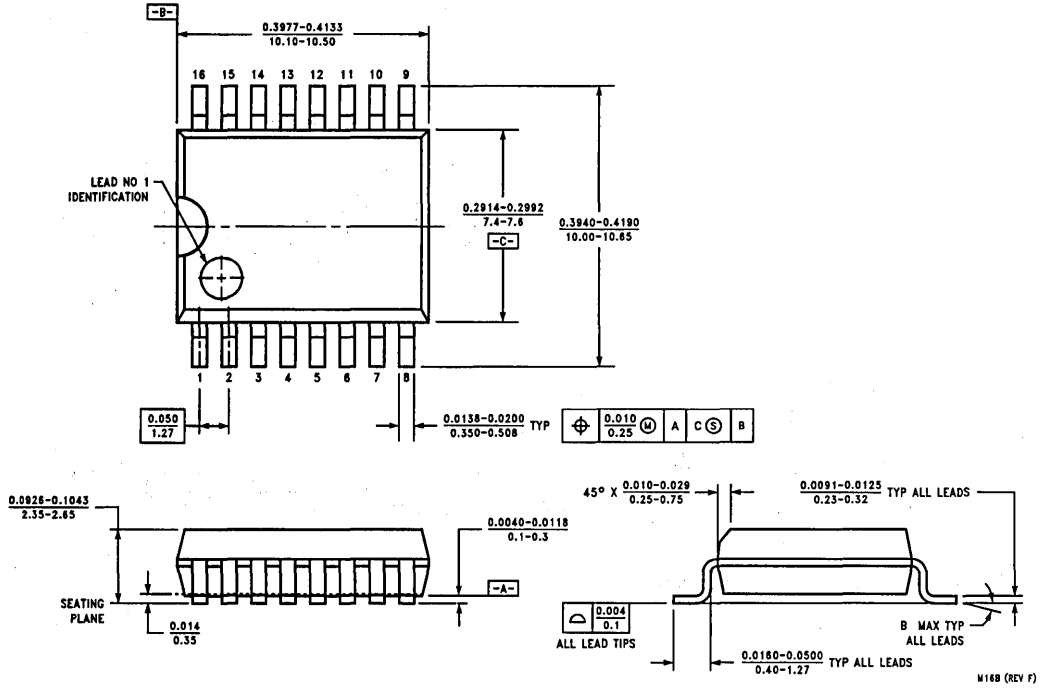
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A



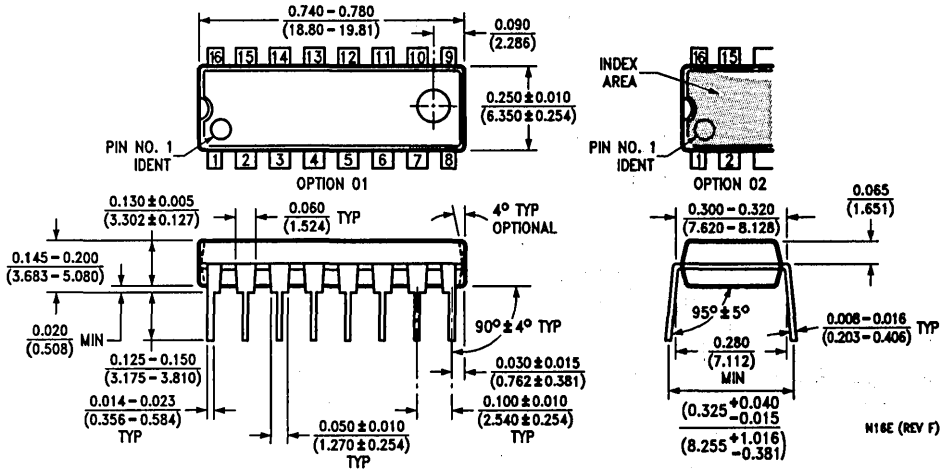
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A



16 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B



16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16E



20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20A