SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated n-p-n power transistors in a TO-3 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

QUICK REFERENCE DATA

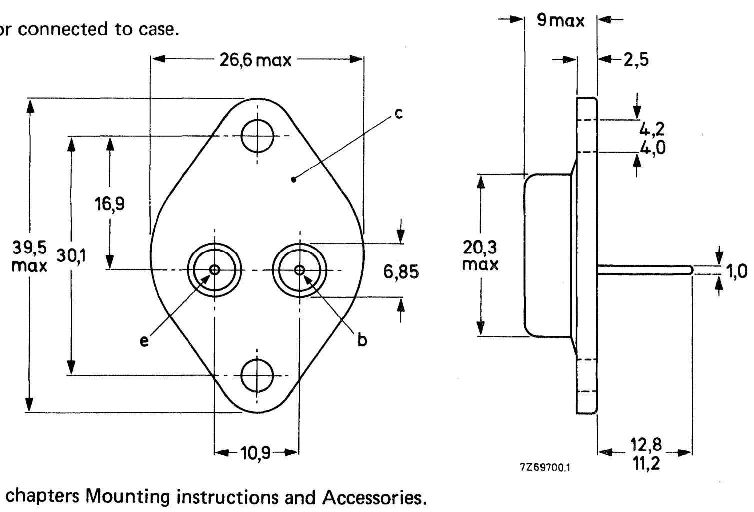
			BUS12	BUS12A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8	8	A
Collector current (peak value) $t_p \leq 2$ ms	I_{CM}	max.	20	20	A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125	125	W
Collector-emitter saturation voltage					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
Fall time (resistive load)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A	t_f	<	0,8	–	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A	t_f	<	–	0,8	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Collector connected to case.



See also chapters Mounting instructions and Accessories.

Products approved to CECC50 004-106 available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUS12	BUS12A	
Collector-emitter voltage (V_{BE} = 0, peak value)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (d.c.)	I_C	max.	8		A
Collector current (peak value); $t_p < 2$ ms	I_{CM}	max.	20		A
Base current (d.c.)	I_B	max.	4		A
Base current (peak value); $t_p \leqslant 2$ ms	I_{BM}	max.	6		A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125		W
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,4	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current *				
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$	I_{CES}	<	1	mA
$V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; T_j = 125 °C	I_{CES}	<	3	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 9$ V	I_{EBO}	<	10	mA

			BUS12	BUS12A	
Saturation voltages					
I_C = 6 A; I_B = 1,2 A	V_{CEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{CEsat}	<	–	1,5	V
I_C = 6 A; I_B = 1,2 A	V_{BEsat}	<	1,5	–	V
I_C = 5 A; I_B = 1 A	V_{BEsat}	<	–	1,5	V
Collector-emitter sustaining voltage					
I_C = 100 mA; I_{Boff} = 0; L = 25 mH	$V_{CEOsust}$	>	400	450	V

* Measured with a half sine-wave voltage (curve tracer).

CHARACTERISTICS (continued)

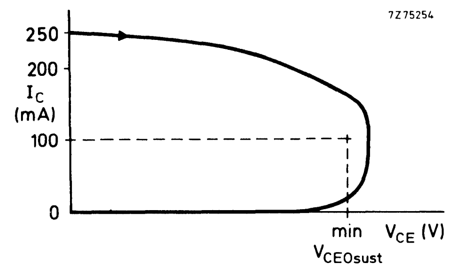


Fig. 2 Oscilloscope display for sustaining voltage.

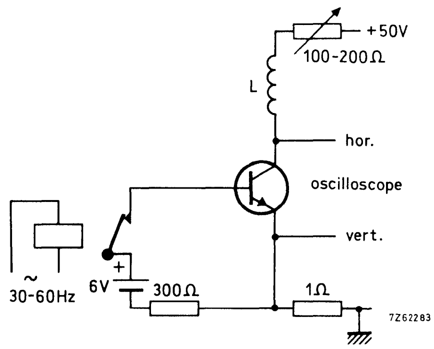


Fig. 3 Test circuit for $V_{CEOsust}$.

			BUS12	BUS12A	
Switching times resistive load (Figs 4 and 5)					
I_{Con} = 6 A; I_{Bon} = $-I_{Boff}$ = 1,2 A					
Turn-on time	t_{on}	<	1	–	μs
Turn-off: Storage time	t_s	<	4	–	μs
Fall time	t_f	<	0,8	–	μs
I_{Con} = 5 A; I_{Bon} = $-I_{Boff}$ = 1 A					
Turn-on time	t_{on}	<	–	1	μs
Turn-off: Storage time	t_s	<	–	4	μs
Fall time	t_f	<	–	0,8	μs
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 6 A; I_B = 1,2 A					
Turn-off: Storage time	t_s	typ.	1,6	–	μs
		<	2,1	–	μs
Fall time	t_f	typ.	80	–	ns
		<	150	–	ns
I_{Con} = 6 A; I_B = 1,2 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	1,8	–	μs
		<	2,3	–	μs
Fall time	t_f	typ.	140	–	ns
		<	300	–	ns
Switching times inductive load (Figs 6 and 7)					
I_{Con} = 5 A; I_B = 1 A					
Turn-off: Storage time	t_s	typ.	–	1,6	μs
		<	–	2,1	μs
Fall time	t_f	typ.	–	80	ns
		<	–	150	ns
I_{Con} = 5 A; I_B = 1 A; T_j = 100 °C					
Turn-off: Storage time	t_s	typ.	–	1,8	μs
		<	–	2,3	μs
Fall time	t_f	typ.	–	140	ns
		<	–	300	ns

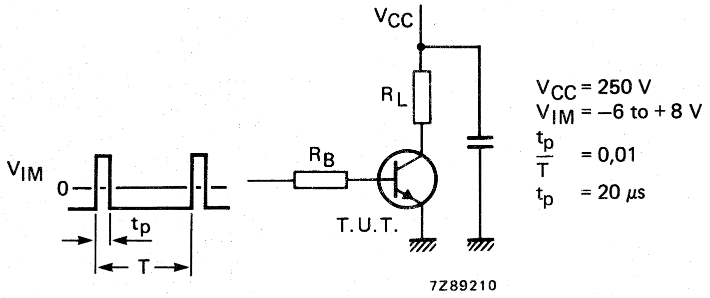


Fig. 4 Test circuit resistive load.

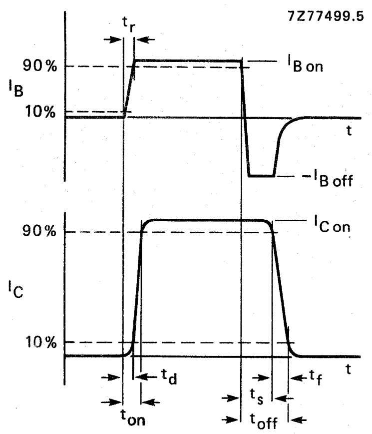


Fig. 5 Switching times waveforms with resistive load.

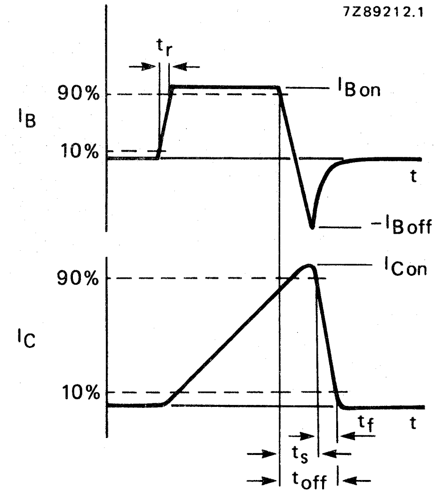


Fig. 6 Switching times waveforms with inductive load.

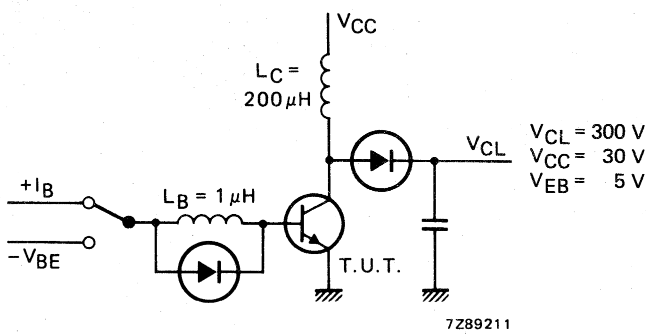
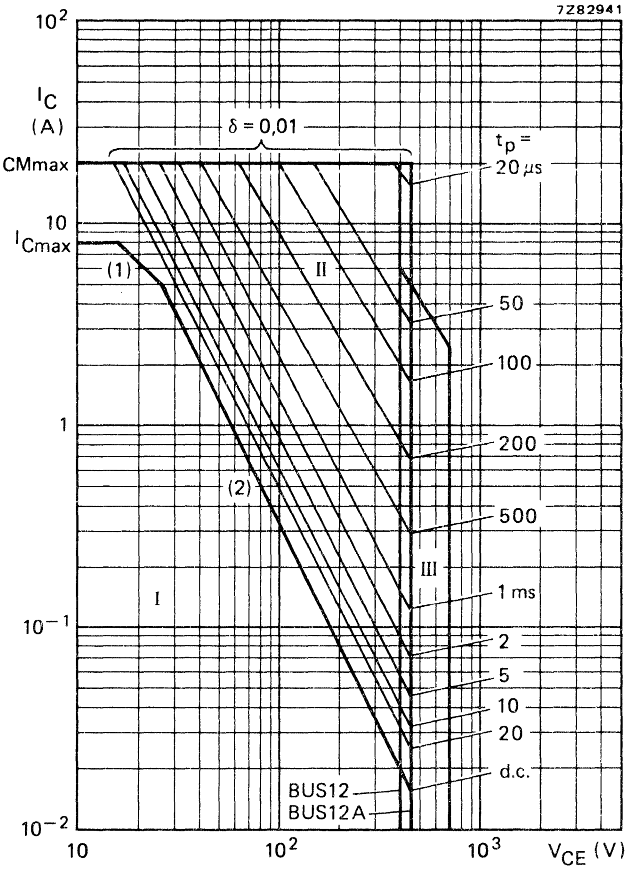


Fig. 7 Test circuit inductive load.



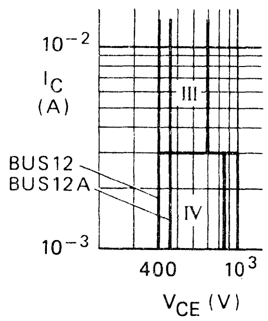


Fig. 8 Safe Operating ARea at $T_{mb} \leq 25$ °C.

(1) $P_{tot\ max}$ and $P_{tot\ peak\ max}$ lines.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0,6\ \mu s$.
IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leq 0$ and $t_p \leq 2$ ms.

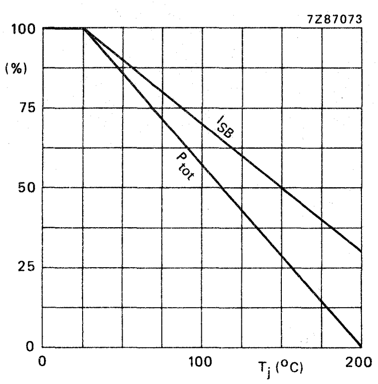


Fig. 9 Total power dissipation and second-breakdown current derating curve.

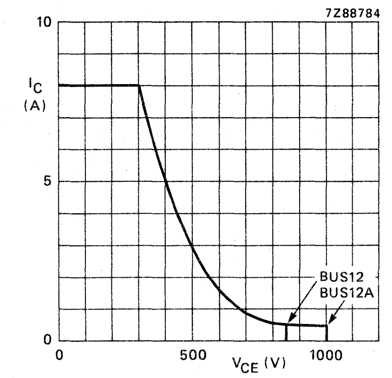


Fig. 10 Reverse bias SOAR.

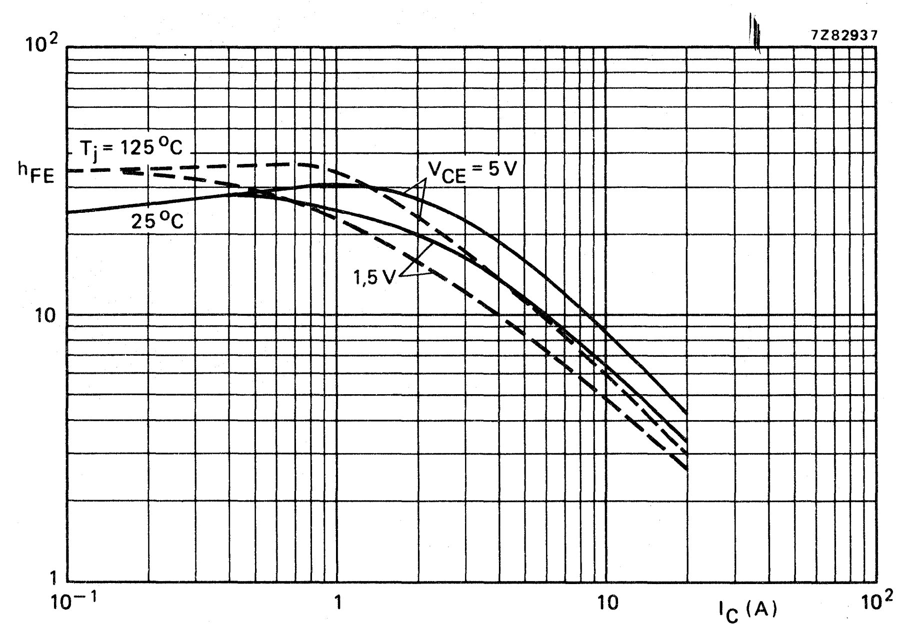


Fig. 11 Typical values d.c. current gain.

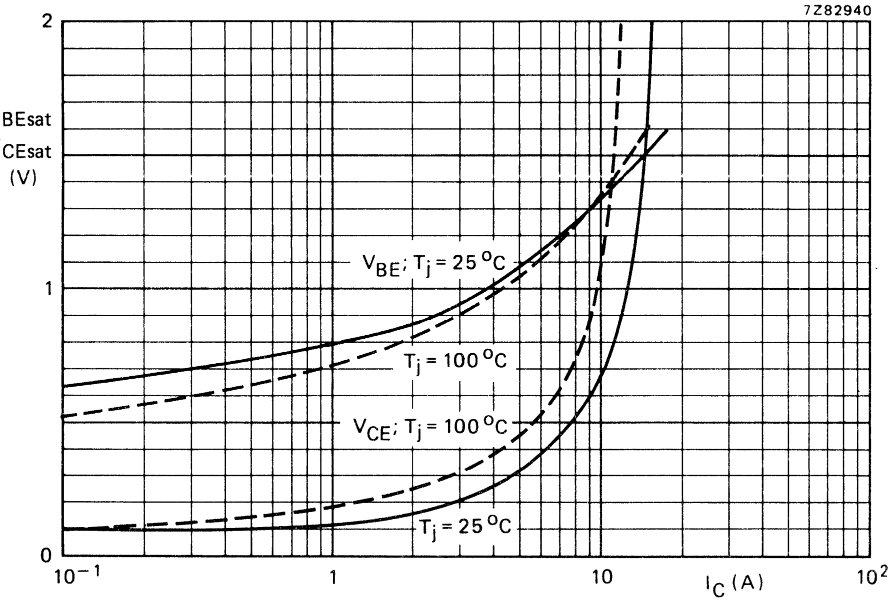


Fig. 12 Typical values base and collector voltage at $I_C/I_B = 5$.

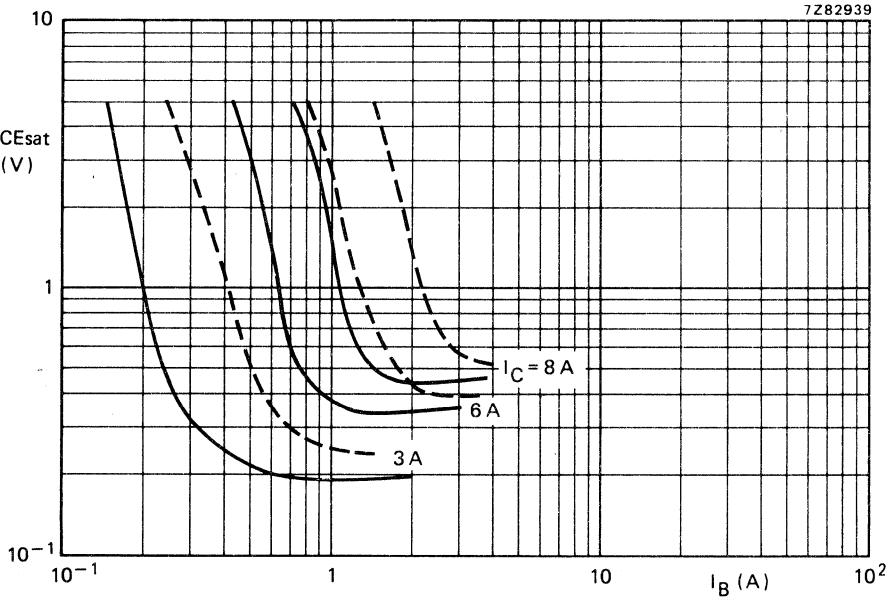


Fig. 13 Typ. (——) and max. (– – –) values collector-emitter saturation voltage at T_j = 25 °C.

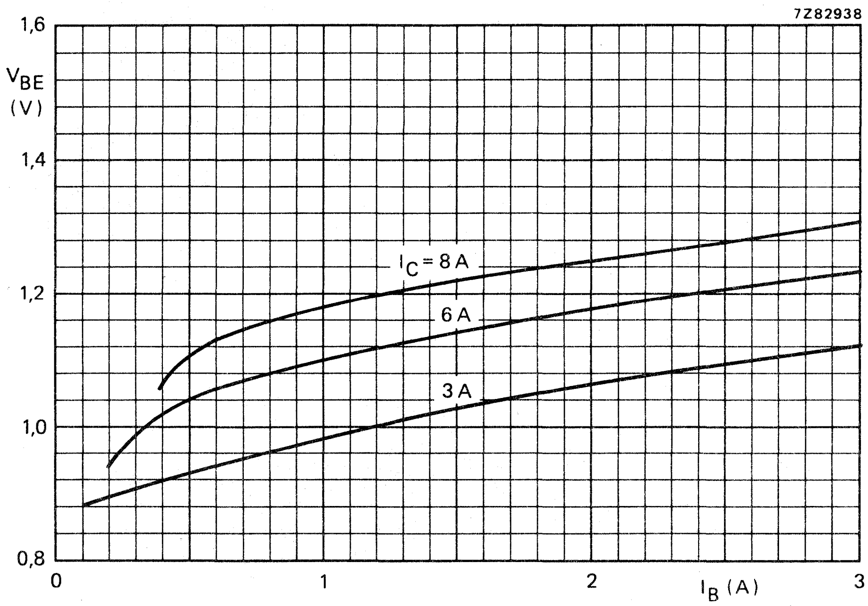


Fig. 14 Typical values base-emitter voltage at T_j = 25 °C.

APPLICATION INFORMATION

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in Figs 15, 16 and 17. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 15):

– collector current shape I_{C1}/I_{CM} = 0,9
– duty factor t_p/T = 0,45
– rate of rise of I_C during turn-on = 8 A/µs
– rate of rise of V_{CE} during turn-off = 1 kV/µs
– reverse drive voltage during turn-off = 5 V
– base current shape I_{B1}/I_{Be} = 1,5

The required thermal resistance of the heatsink can be calculated from

$$R_{th\ mb\text{-}a} < \frac{100 - T_{amb}}{P_{tot}} \quad \text{K/W}$$

To ensure thermal stability the value of the ambient temperature $T_{amb} > 40$ °C.

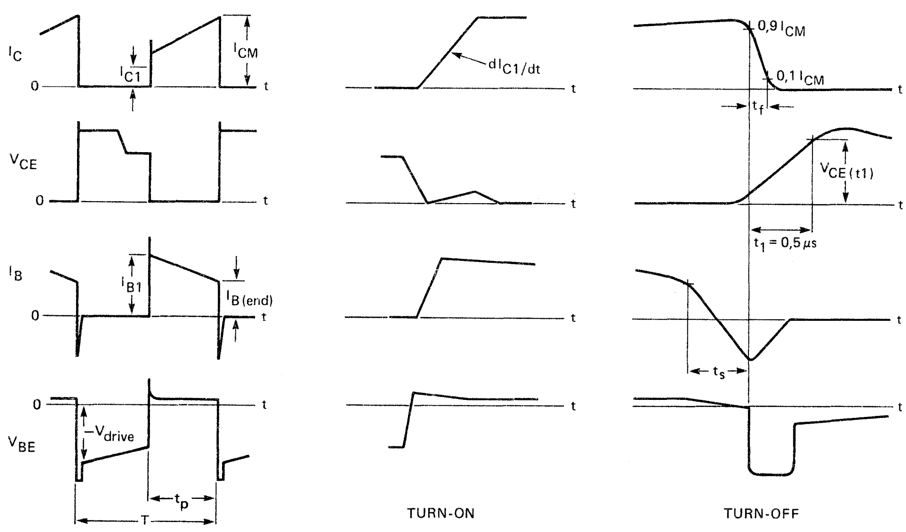


Fig. 15 Relevant waveforms of the switching transistor in a forward SMPS.

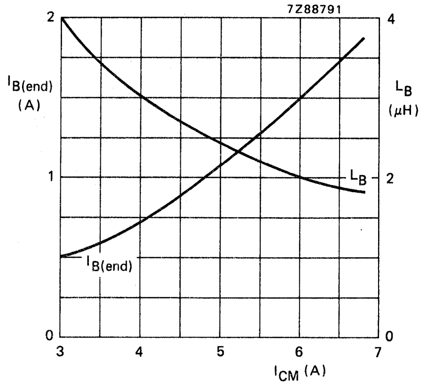


Fig. 16 Recommended nominal "end" value of the base current (I_{Be}) and optimum base inductance (L_B) at $-V_{drive}$ = 5 V versus maximum peak collector current. $dI_{B(end)}$ = ± 20%.

For other values of $-V_{drive}$ (3 V to 7 V) the related L_B is:

$$L_{Bnom} \frac{(-V_{drive}) + 1}{6}$$

L_{Bnom} is the value given in this graph.

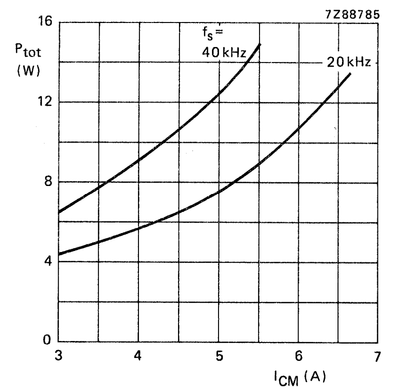


Fig. 17 Maximum transistor dissipation under worse-case operating condition versus maximum peak collector current. T_{mb} = 100 °C; $dI_{B(end)}$ = ± 20%.