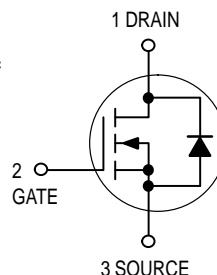


Logic Level TMOS N-Channel Enhancement Mode

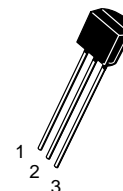
This TMOS FET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

- Low Drive Requirement, $V_{GS} = 3.0\text{ V max}$
- Inherent Current Sharing Capability Permits Easy Paralleling of many Devices



BS108

**200 VOLTS
N-CHANNEL TMOS
POWER FET
LOGIC LEVEL**



**CASE 29-04, STYLE 30
TO-92**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current Continuous(1) Pulsed(2)	I_D I_{DM}	250 500	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $T_A = 25^\circ\text{C}$	P_D	350 6.4	mW mW/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

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BS108

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0, I _D = 10 μA)	V _{(BR)DSS}	200	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DSS} = 130 Vdc, V _{GS} = 0)	I _{DSS}	—	—	30	nAdc
Gate–Body Leakage Current (V _{GS} = 15 Vdc, V _{DS} = 0)	I _{GSSF}	—	—	10	nAdc
ON CHARACTERISTICS (2)					
Gate Threshold Voltage (I _D = 1.0 mA, V _{DS} = V _{GS})	V _{GS(th)}	0.5	—	1.5	Vdc
Static Drain–to–Source On–Resistance (V _{GS} = 2.0 Vdc, I _D = 50 mA) (V _{GS} = 2.8 Vdc, I _D = 100 mA)	r _{DS(on)}	— —	— —	10 8.0	Ohms
Drain Cutoff Current (V _{GS} = 0.2 V, V _{DS} = 70 V)	I _{DSX}	—	—	25	μA
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	—	—	150	pF
Output Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{oss}	—	—	30	pF
Reverse Transfer Capacitance (V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	—	—	10	pF
SWITCHING CHARACTERISTICS					
Turn–On Time (See Figure 1)	t _{d(on)}	—	—	15	ns
Turn–Off Time (See Figure 1)	t _{d(off)}	—	—	15	ns

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

RESISTIVE SWITCHING

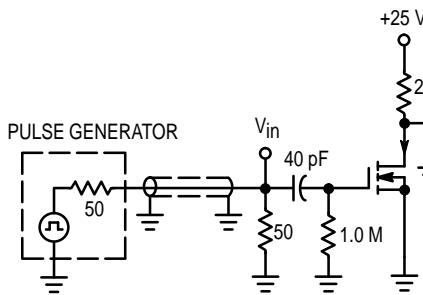


Figure 1. Switching Test Circuit

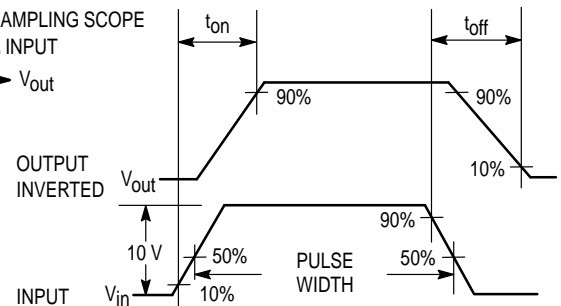
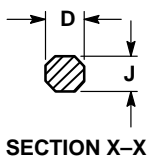
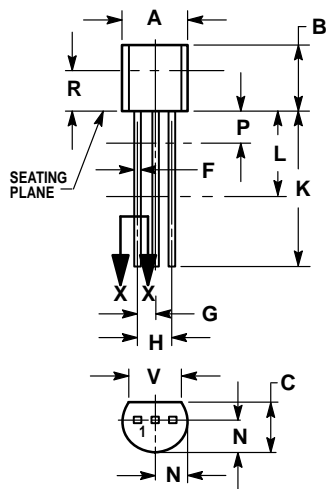


Figure 2. Switching Waveforms

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

STYLE 30:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 029-04
 (TO-226AA)
 ISSUE AD**

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