Am27S32 • Am27S33

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S32 and Am27S33 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

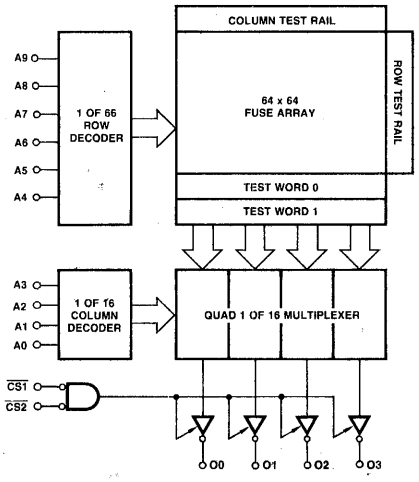
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S32DC
Hermetic DIP	−55°C to +125°C	AM27S32DM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S33DC
Hermetic DIP	−55°C to 125°C	AM27S33DM

FUNCTIONAL DESCRIPTION

The Am27S32 and Am27S33 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 4 configuration, they are available in both open collector Am27S32 and three-state Am27S33 output versions. After programming, stored information is read on outputs O0–O3 by applying unique binary addresses to A0–A9 and holding the chip select inputs, $\overline{CS1}$ and $\overline{CS2}$, LOW. If either chip select input goes to a logic HIGH, O0–O3 go to the off or high impedance state.

BLOCK DIAGRAM



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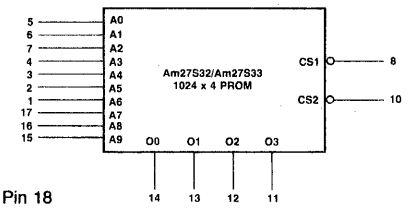
LOGIC SYMBOL



VCC = Pin 18
GND = Pin 9

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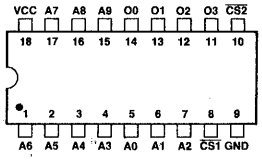
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +VCC max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S32XC, Am27S33XC	T_A = 0°C to +75°C	VCC = 5.0V ±5%
MIL	Am27S32XM, Am27S33XM	T_A = −55°C to +125°C	VCC = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
VOH (Am27S33 only)	Output HIGH Voltage	VCC = MIN., IOH = −2.0mA VIN = VIH or VIL			2.4			Volts
VOL	Output LOW Voltage	VCC = MIN., IOL = 16mA VIN = VIH or VIL					0.45	Volts
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.45V				−0.020	−0.250	mA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V					25	μA
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
ISC (Am27S33 only)	Output Short Circuit Current	VCC = MAX., VOUT = 0.0V (Note 2)			−20	−40	−90	mA
ICC	Power Supply Current	All inputs = GND VCC = MAX.		COM'L		105	140	mA
				MIL		105	145	
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.2	Volts
ICEX	Output Leakage Current	VCC = MAX. $\overline{VCS1}$ = 2.4V		VO = 4.5V			40	μA
			Am27S33 only	VO = 2.4V			40	
				VO = 0.4V			−40	
CIN	Input Capacitance	VIN = 2.0V @ f = 1MHz (Note 3)				5		pF
COUT	Output Capacitance	VOUT = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at VCC = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

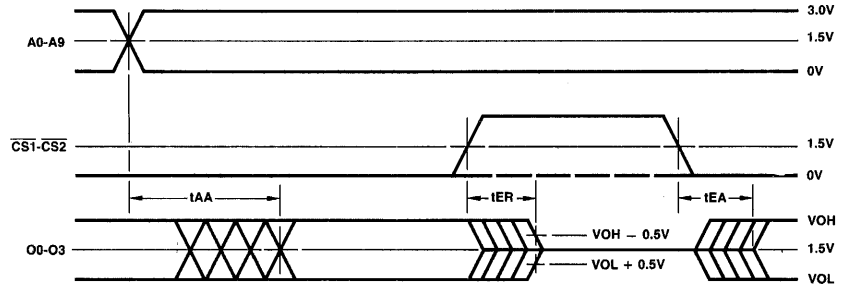
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	38	55	70	ns
t_{EA}	Enable Access Time		10	25	30	ns
t_{ER}	Enable Recovery Time		10	25	30	ns

Notes: 1. tAA is tested with switch S1 closed and CL = 30pF.
2. For open collector outputs, tEA and tER are tested with S1 closed to the 1.5V output level. CL = 30pF.
3. For three state outputs, tEA is tested with CL = 30pF to the 1.5V level; S1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. tER is tested with CL = 5pF. HIGH to high impedance tests are made with S1 open to an output voltage of VOH − 0.5V; LOW to high impedance tests are made with S1 closed to the VOL + 0.5V level.

SWITCHING CHARACTERISTICS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

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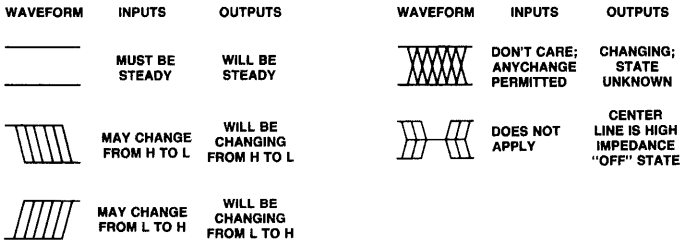
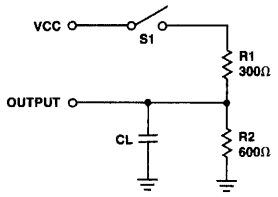
KEY TO TIMING DIAGRAM



AC TEST LOAD



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PROGRAMMING

The Am27S32 and Am27S33 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including VCC should be removed for a period of 5 seconds after which programming may be resumed.

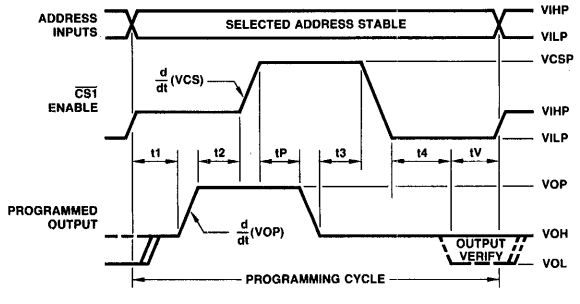
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
VCCP	VCC During Programming	5.0	5.5	Volts
VIHP	Input HIGH Level During Programming	2.4	5.5	Volts
VILP	Input LOW Level During Programming	0.0	0.45	Volts
VCSP	$\overline{CS1}$ Voltage During Programming	14.5	15.5	Volts
VOP	Output Voltage During Programming	19.5	20.5	Volts
VONP	Voltage on Outputs. Not to be Programmed	0	VCCP+0.3	Volts
IONP	Current into Outputs Not to be Programmed		20	mA
d(VOP)/dt	Rate of Output Voltage Change	20	250	V/μsec
d(VCS)/dt	Rate of $\overline{CS1}$ Voltage Change	100	1000	V/μsec
tP	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e. not to the midpoints.
2. Delays t1, t2, t3 and t4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During tv, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to VONP through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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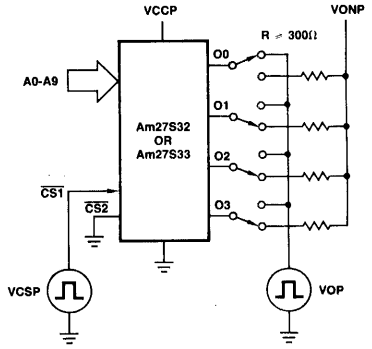
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each base part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S32 • Am27S33 ADAPTERS AND CONFIGURATOR	715-1414	PA 18-6 and 1024 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 1024 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

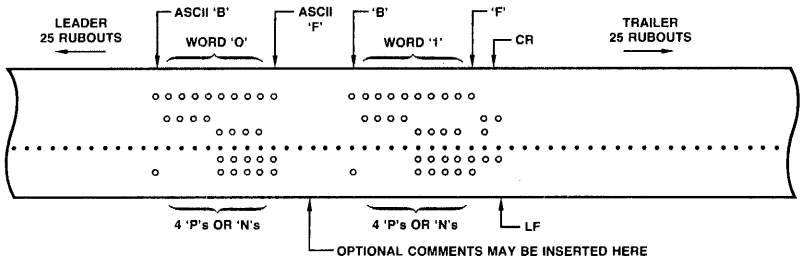
ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
ØØ2	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
ØØ4	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
ØØ6	BPPNNF	HERE (R) (L)
•	•••••••	•
•	•••••••	•
1024	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE

($\overline{CS1}$ and $\overline{CS2}$ = LOW)

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O3	O2	O1	O0
L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	H	H	L	H	H	L	L
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	H	H	H	H	H	H	H	H	H	H	H	H	L

ASCII PAPER TAPE



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