Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

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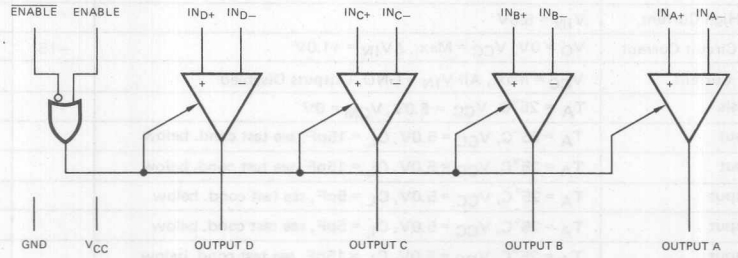
LOGIC DIAGRAM



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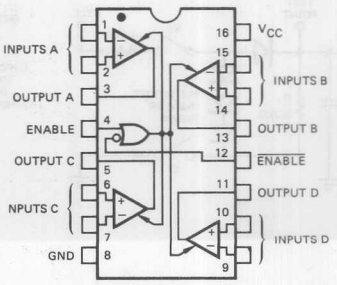
ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	–55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	–55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	–55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

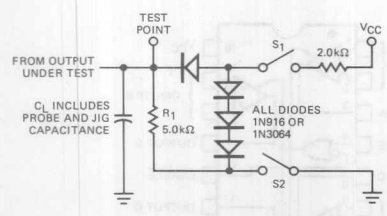
The following conditions apply unless otherwise specified:

Am26LS32XM, Am26LS33XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$
Am26LS32XC, Am26LS33XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, $-7V \leq V_{CM} \leq +7V$	0.2	0.06	0.2	Volts
			Am26LS33, $-15V \leq V_{CM} \leq +15V$	0.5	0.12	0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0k	8.5k		Ω
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0V$	COM'L	2.7	3.4		Volts
		$V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0V$	$I_{OL} = 4.0mA$			0.4	Volts
		$V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$			0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5V$			1	100	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max., $\Delta V_{IN} = +1.0V$		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



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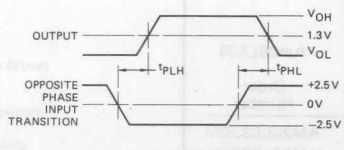
PROPAGATION DELAY (Notes 1 and 3)



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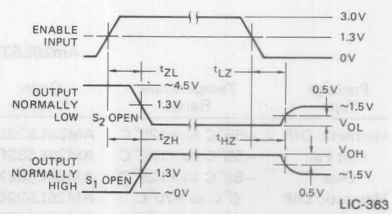
ENABLE AND DISABLE TIMES (Notes 2 and 3)



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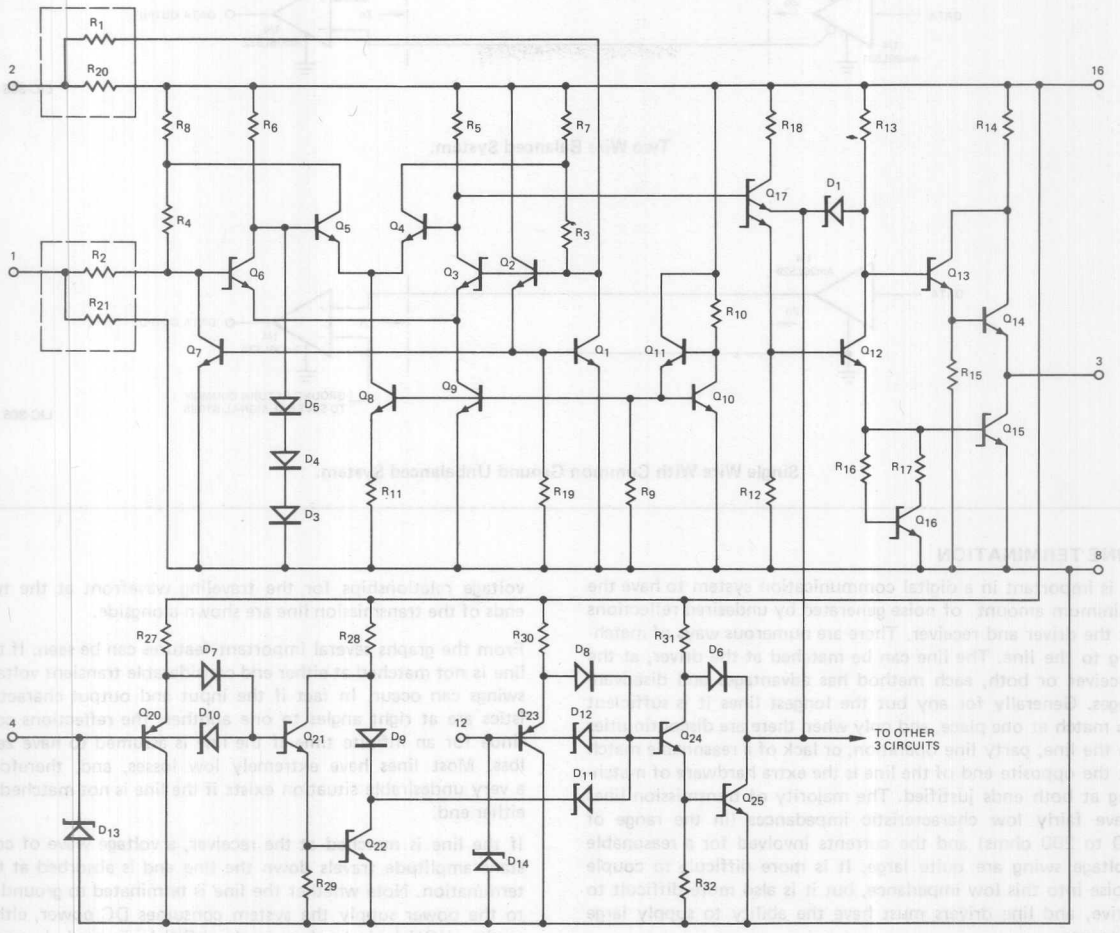
Notes:
1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

EQUIVALENT CIRCUIT (1/4 Am26LS32 OR Am26LS33)



Note: R_3 and R_4 value for Am26LS32 is 2 times Am26LS33 value.

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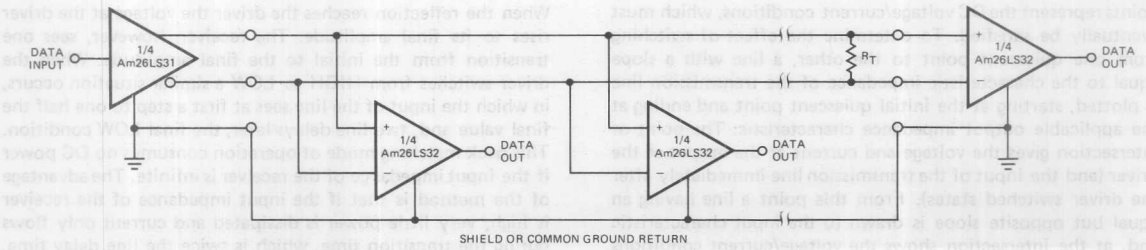
TYPICAL APPLICATION



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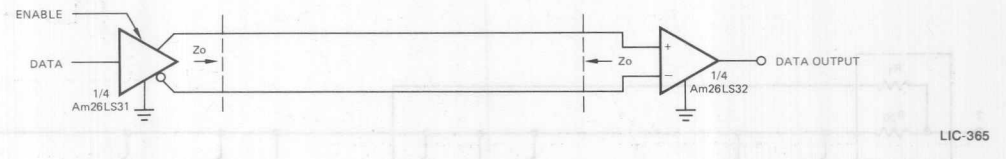
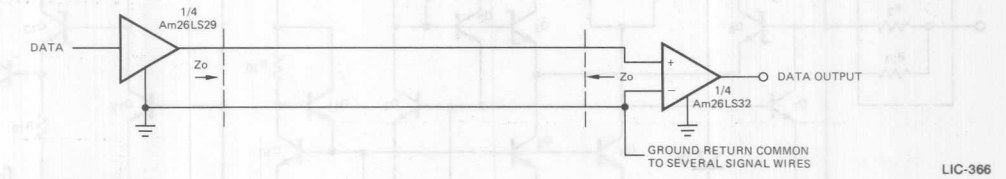


Two Wire Balanced System.



Single Wire With Common Ground Unbalanced System.

LINE TERMINATION

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of a reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

Various matching techniques that can be employed are shown in Figure 1. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V-I graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points — points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switched states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees one transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line sees at first a step to one half the final value and, two line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.

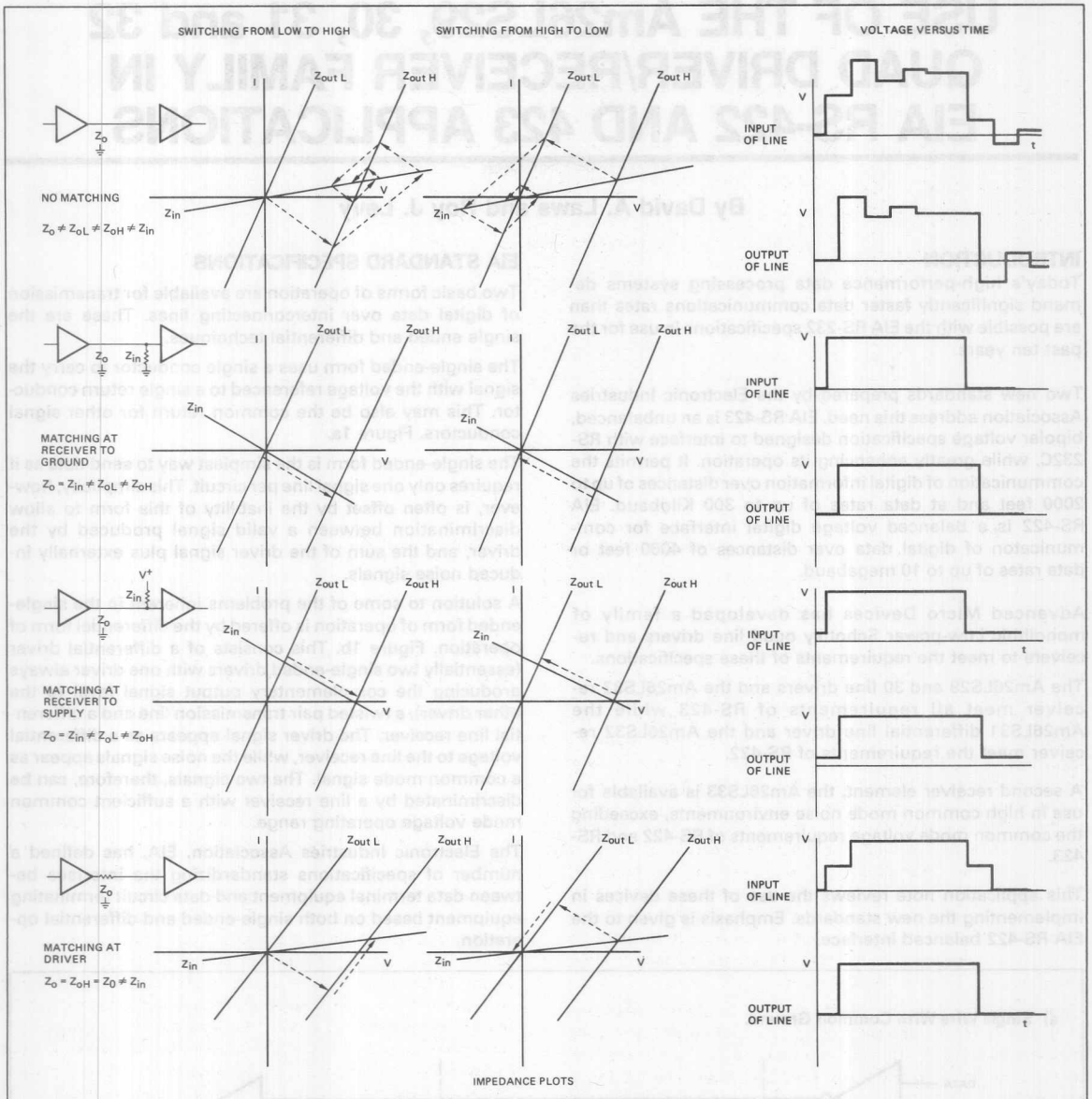
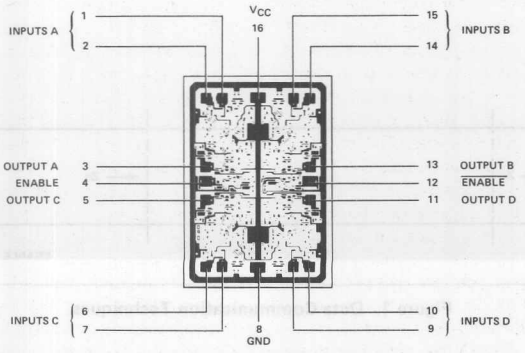


Figure 1. Line Matching Methods LIC-367

Metallization and Pad Layout



DIE SIZE
0.087" X 0.059"