LPTTL/MONOSTABLE 96L02
LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 96L02 is a low power Dual Retriggerable, Resettable Monostable Multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

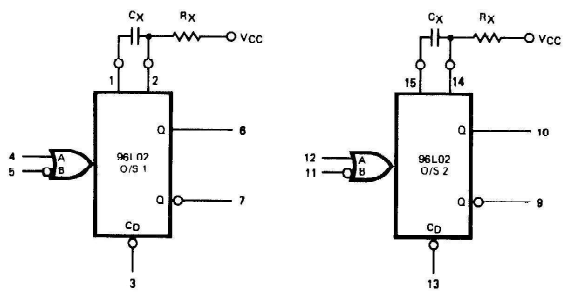
- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

PIN NAMES

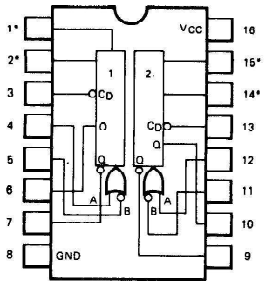
		LOADING HIGH	LOADING LOW
$\overline{B}$	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
$\overline{C}_D$	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
$\overline{Q}$	Output (Active LOW)	9.0	3.0

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

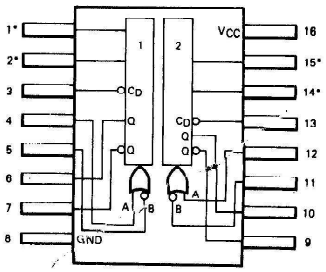


CONNECTION DIAGRAMS
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)

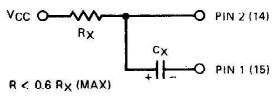


*Pins for external timing.

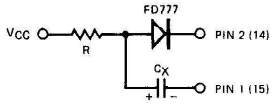
FUNCTIONAL DESCRIPTION — The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active level LOW input or the Q output to the active level HIGH input.

OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for −55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:
$$t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right] \text{ (for } C_X > 10^3 \text{ pF)}$$
Where R_X is in kΩ, C_X is in pF, t is in ns. For $C_X < 10^3$ pF, see Fig. 1
5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 μA, and the inverse capacitor leakage at 1.0 V is less than 1.6 μA over the operational temperature range and Rule 3 above is satisfied.

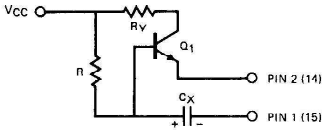


   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



$$t \approx 0.3\ RC_X$$

   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



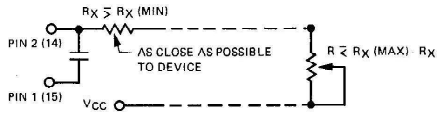
$R < R_X\,(0.7)\,(h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
R_X (min) $< R_Y < R_X$ (max)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\ RC_X$$

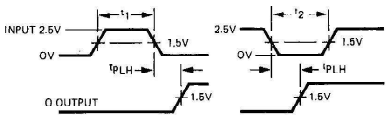
This configuration is not recommended with retriggerable operation.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

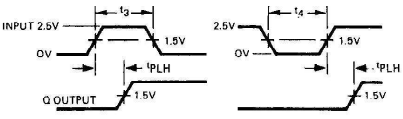


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

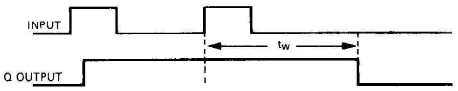
Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH
t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
t_2, t_4 = Min. Negative Input Pulse Width > 60 ns



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH

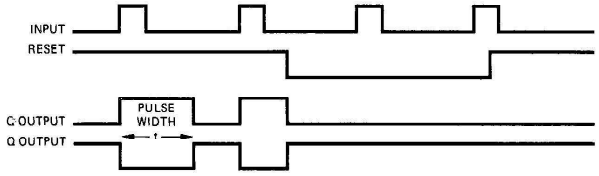


9. The retriggerable pulse width is calculated as shown below:
$$t_W = t + t_{PLH} = 0.33\ R_X C_X \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation — An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
96L02XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		Volts	V_{CC} = MIN., I_{OH} = −0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−2.0		−13	mA	V_{CC} = MAX., V_{OUT} = 1.0 V
I_{CC}	Power Supply Current		10	16	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
96L02XM						
t_{PLH}	Negative Trigger Input to True Output		55	75	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output		45	62	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width		110		ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t	Pulse Width	12.4	13.8	15.2	μs	V_{CC} = 5.0 V, R_X = 39 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	R_X = 39 kΩ, C_X = 1000 pF
96L02XC						
t_{PLH}	Negative Trigger Input to True Output		55	80	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output		45	65	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width		110		ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t	Pulse Width	12.4	13.8	15.2	μs	V_{CC} = 5.0 V, R_X = 39 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	R_X = 39 kΩ, C_X = 1000 pF

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X ($C_X \leq$ 1000 pF)
(FOR C_X > 1000 pF SEE OPERATION RULES 4 AND 5.)

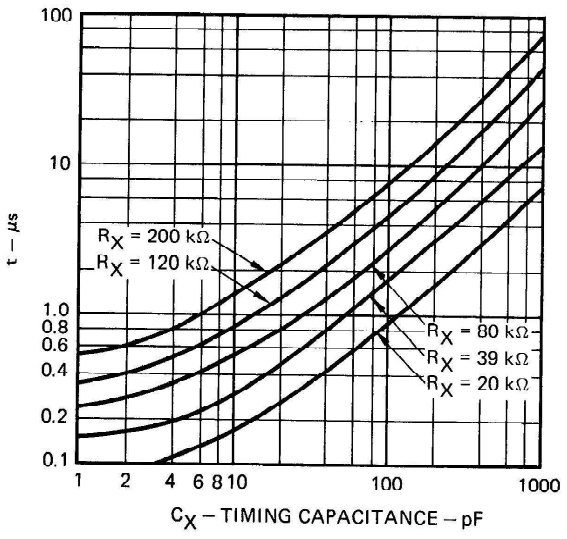
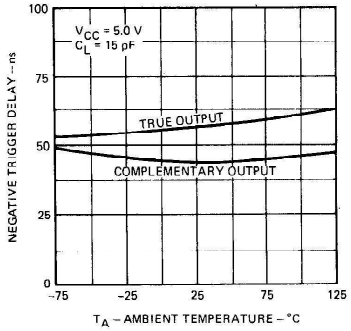


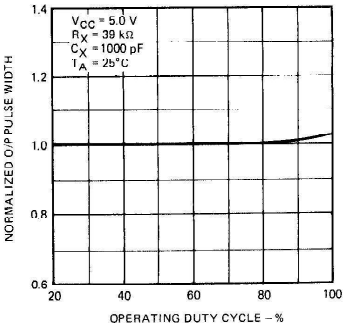
Fig. 1

TYPICAL PULSE CHARACTERISTICS

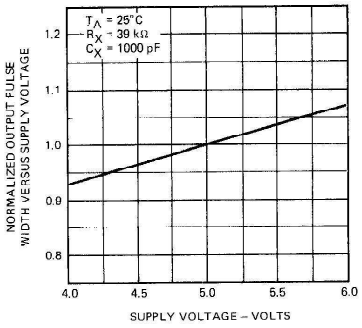
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



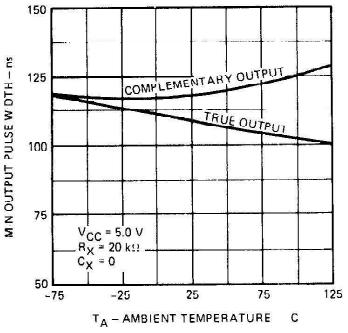
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



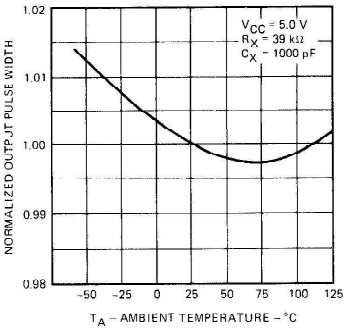
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MIN. OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

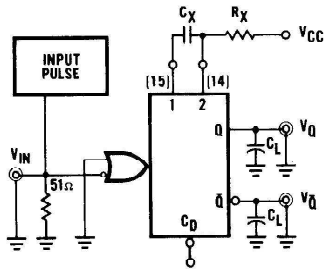


TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Don't Care (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns