54LS/74LS670

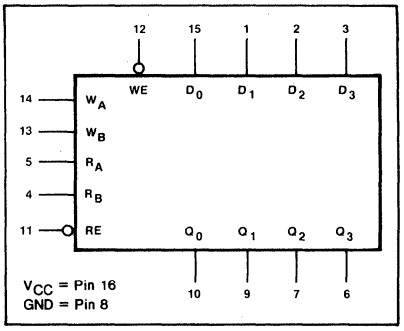
DESCRIPTION

The "670" is a 4-by-4 Register File with 3-State outputs organized as 4-words of 4-bits. Simultaneous read and write operation is allowed by separate read and write inputs, both address and enable. An almost unlimited number of devices can be stacked to increase the word capacity by tying the 3-state outputs together. Any number of these devices can be operated in parallel to generate an n-bit word.

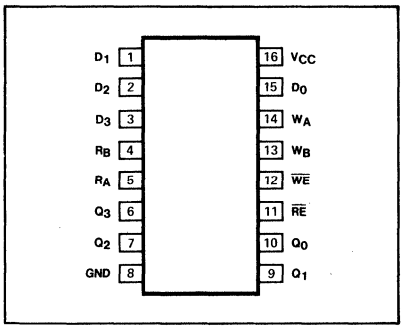
FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-State outputs**
- **See "170" for open collector version**

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +70°C	MILITARY RANGES V_{CC}=5V±10%; T_A=−55°C to +125°C
Plastic DIP	N74LS670N	
Ceramic DIP	N74LS670F	S54LS670F
Flatpak		S54LS670W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE[a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D_0-D_3	Data inputs	I_{IH} (μA) I_{IL} (mA)			20 −0.4
W_A, W_B	Write address inputs	I_{IH} (μA) I_{IL} (mA)			20 −0.4
$\overline{WE}$	Write Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 −0.8
R_A, R_B	Read address inputs	I_{IH} (μA) I_{IL} (mA)			20 −0.4
$\overline{RE}$	Read Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 −0.8
Q_0-Q_3	Outputs	I_{OH} (mA) I_{OL} (mA)			−1/−2.6[a] 4/8[a]

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[d]

PARAMETER		TEST CONDITIONS		54/74 Min	54/74 Max	54S/74S Min	54S/74S Max	54LS/74LS Min	54LS/74LS Max	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} =−1.0mA					2.4		V
			I_{OH} =−2.6mA					2.4[e]		V
I_{CC}	Supply current	V_{CC} = Max							50	mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

d. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

e. This parameter for Commercial range only.

FUNCTIONAL DESCRIPTION

The "670" is a 16-bit 3-State Register File organized as 4-words of 4-bits each. Separate read and write address and enable inputs are available permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_A & W_B) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A & R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is LOW. Data outputs are in the high impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[b]
	$\overline{WE}$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE

b. The Write Address (W_A & W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	INTERNAL LATCHES[c]	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE

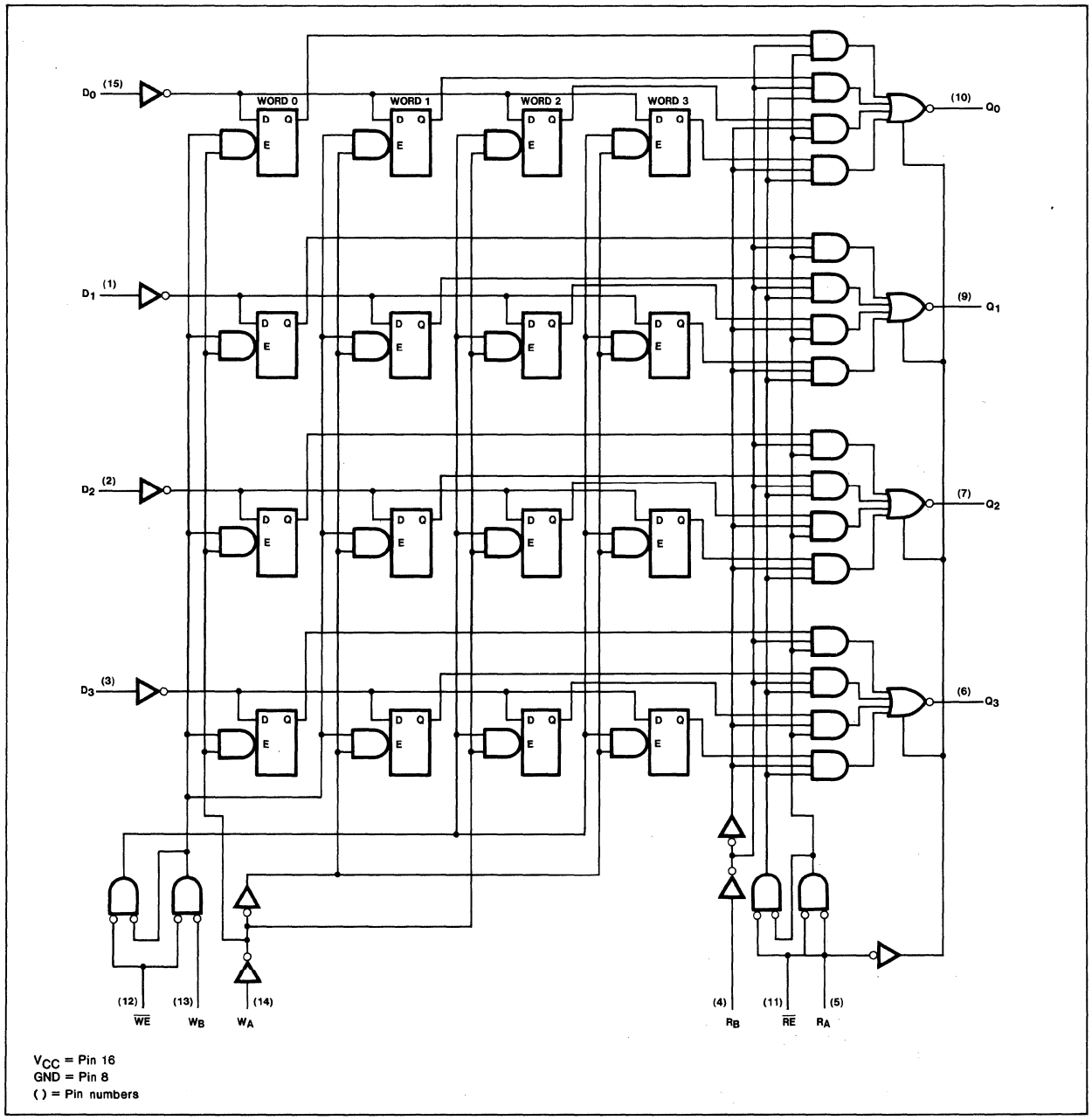
c. The Read Address (R_A & R_B) changes to select the "internal latches" are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" state

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
							C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Figure 2						40	ns
t_{PHL}	Read Address to output							45	ns
t_{PLH}	Propagation delay	Figure 1						45	ns
t_{PHL}	Write Enable to output							50	ns
t_{PLH}	Propagation delay	Figure 1						45	ns
t_{PHL}	Data to output							40	ns
t_{PZH}	Read enable time to HIGH level	Figure 4						35	ns
t_{PZL}	Read enable time to LOW level	Figure 5						40	ns
t_{PHZ}	Disable time from HIGH level	Figure 4, C_L = 5pF						50	ns
t_{PLZ}	Disable time from LOW level	Figure 5, C_L = 5pF						35	ns

LOGIC DIAGRAM



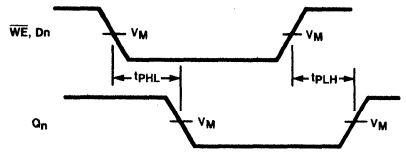
V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
t_W	Write Enable pulse width	Figure 3					25		ns
t_s	Setup time Data to positive going $\overline{WE}$	Figure 3					10		ns
t_h	Hold time Data to positive going $\overline{WE}$	Figure 3					15		ns
t_s	Setup time Read Address to negative going $\overline{WE}$	Figure 3					15		ns
t_h	Hold time Read Adress to positive going $\overline{WE}$	Figure 3					5.0		ns

AC WAVEFORMS

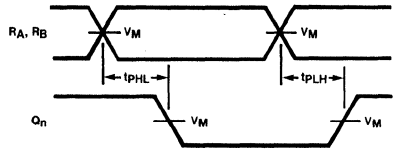
PROPAGATION DELAY, WRITE ENABLE AND DATA TO OUTPUTS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 1

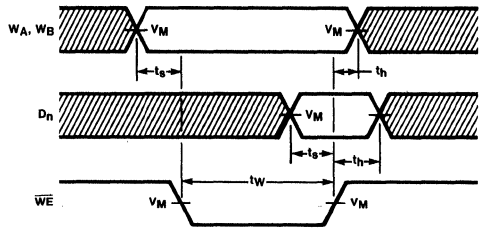
PROPAGATION DELAY READ ADDRESS TO OUTPUTS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 2

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



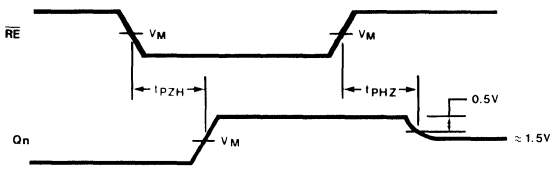
V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3

AC WAVEFORMS (Cont'd

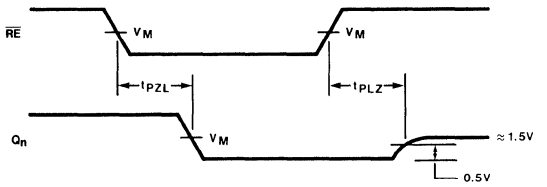
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 4

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 5