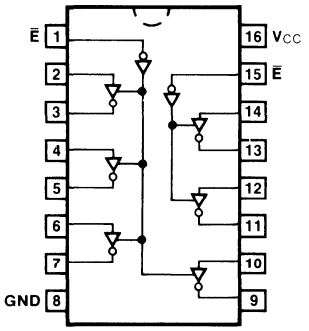
54LS/74LS368A

HEX 3-INPUT INVERTER BUFFER

(With Separate 2-Bit and 4-Bit Sections)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS368APC		9B
Ceramic DIP (D)	A	74LS368ADC	54LS368ADM	6B
Flatpak (F)	A	74LS368AFC	54LS368AFM	4L

TRUTH TABLE

INPUTS $\overline{E}$	INPUTS D	OUTPUT
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	25/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		21	mA	V_{CC} = Max, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay		12 22	ns	Figs. 3-1, 3-5 C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time		24 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.