



## DM74LS293 4-Bit Binary Counter

### General Description

The 'LS293 counter is electrically and functionally identical to the 'LS93. Only the arrangement of the terminals has been changed for the 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

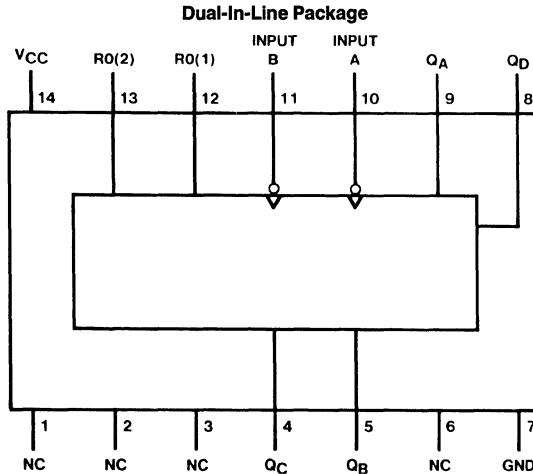
All of these counters have a gated zero reset.

To use the maximum count length (four-bit binary) of these counters, the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

### Features

- GND and  $V_{CC}$  on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

### Connection Diagram



**Order Number DM74LS293M or DM74LS293N**  
**See NS Package Number M14A or N14A**

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**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
DM74LS	
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	DM74LS293			Units
		Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.4	mA
I <sub>OL</sub>	Low Level Output Current			8	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)	A to Q <sub>A</sub>	0	32	MHz
		B to Q <sub>B</sub>	0	16	
f <sub>CLK</sub>	Clock Frequency (Note 2)	A to Q <sub>A</sub>	0	20	MHz
		B to Q <sub>B</sub>	0	10	
t <sub>w</sub>	Pulse Width (Note 6)	A	15		ns
		B	30		
		Reset	15		
t <sub>REL</sub>	Reset Release Time (Note 6)	25			ns
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics** over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.7	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min		0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max V <sub>I</sub> = 7V	Reset		0.1	mA
			A		0.2	
			B		0.2	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V	Reset		20	μA
			A		40	
			B		40	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.4V	Reset		-0.4	mA
			A		-2.4	
			B		-1.6	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 4)	-20		-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 5)		9	15	mA

**Switching Characteristics** at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$t_{MAX}$	Maximum Clock Frequency	A to $Q_A$	32		20		MHz
		B to $Q_B$	16		10		
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_A$		16		23	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_A$		18		30	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_D$		70		87	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_D$		70		93	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_B$		16		23	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_B$		21		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_C$		32		48	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_C$		35		53	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_D$		51		71	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_D$		51		71	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

**Note 1:**  $C_L = 15\text{ pF}$ ,  $R_L = 2\text{ k}\Omega$ ,  $T_A = 25^\circ C$  and  $V_{CC} = 5V$ .

**Note 2:**  $C_L = 50\text{ pF}$ ,  $R_L = 2\text{ k}\Omega$ ,  $T_A = 25^\circ C$  and  $V_{CC} = 5V$ .

**Note 3:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

**Note 4:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 5:**  $I_{CC}$  is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

**Note 6:**  $T_A = 25^\circ C$  and  $V_{CC} = 5V$ .

# Function Tables

Count Sequence (See Note C)

Count	Outputs			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

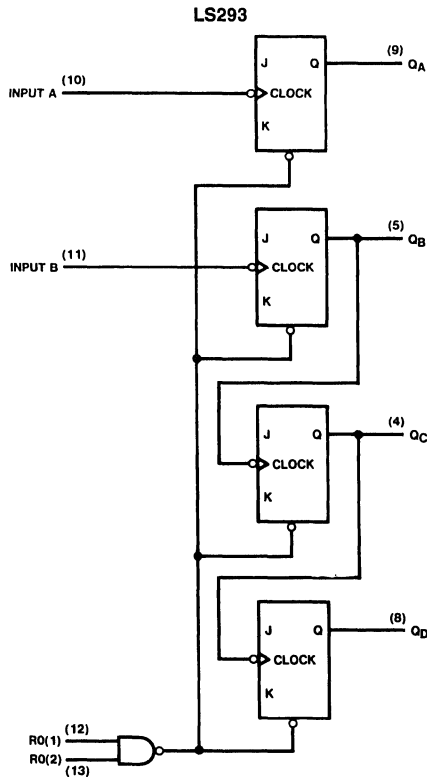
Reset/Count Truth Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H = High Level, L = Low Level, X = Don't Care.

Note C: Output Q<sub>A</sub> is connected to input B.

## Logic Diagram



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Note: The J and K inputs shown without connection are for reference only and are functionally at a high level.